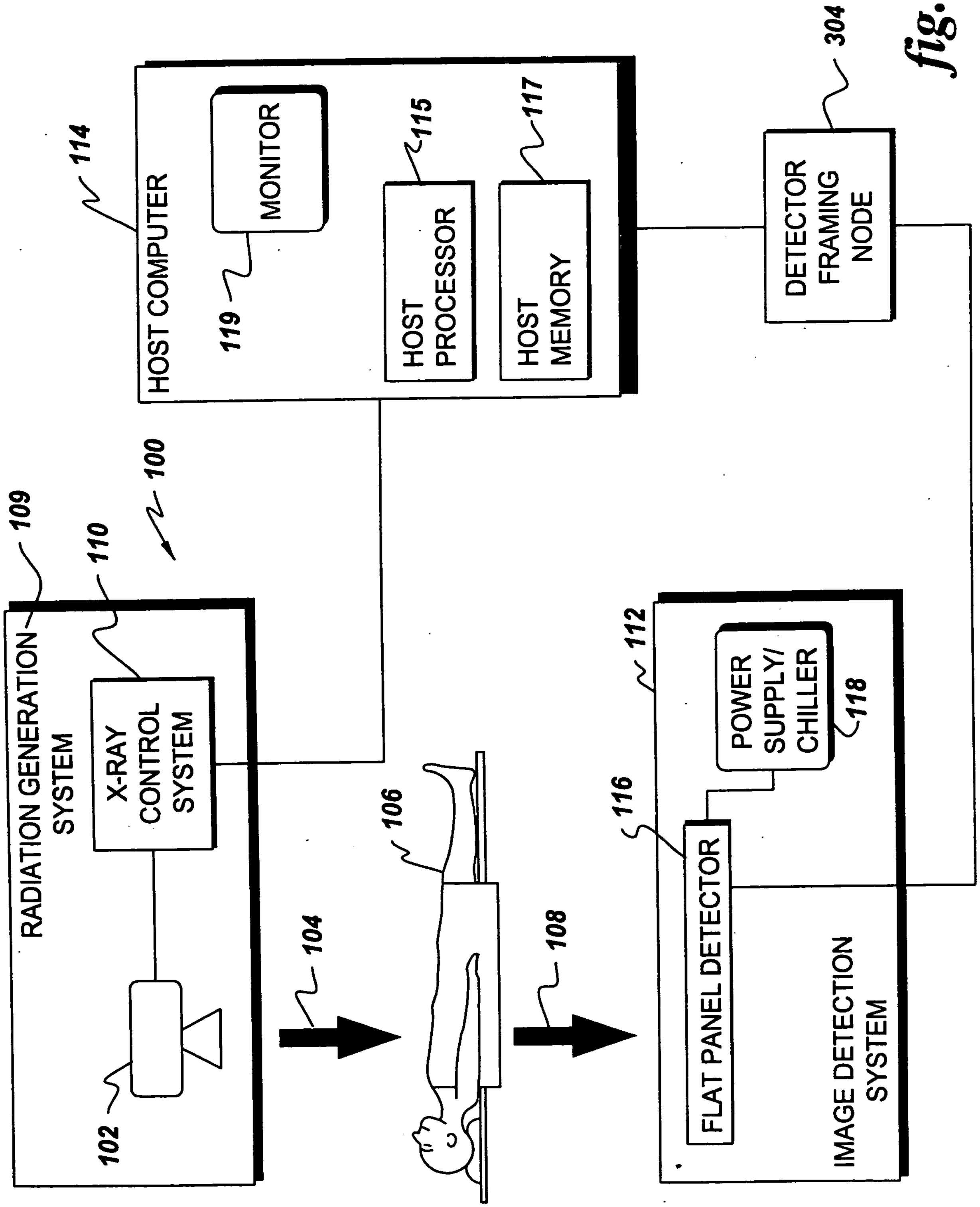

100
RADIATION GENERATION SYSTEM
109
X-RAY CONTROL SYSTEM
110
102
104
106
108
HOST COMPUTER
114
MONITOR
119
HOST PROCESSOR
115
HOST MEMORY
117
DETECTOR FRAMING NODE
304
FLAT PANEL DETECTOR
116
POWER SUPPLY/ CHILLER
118
IMAGE DETECTION SYSTEM
112

fig. 1

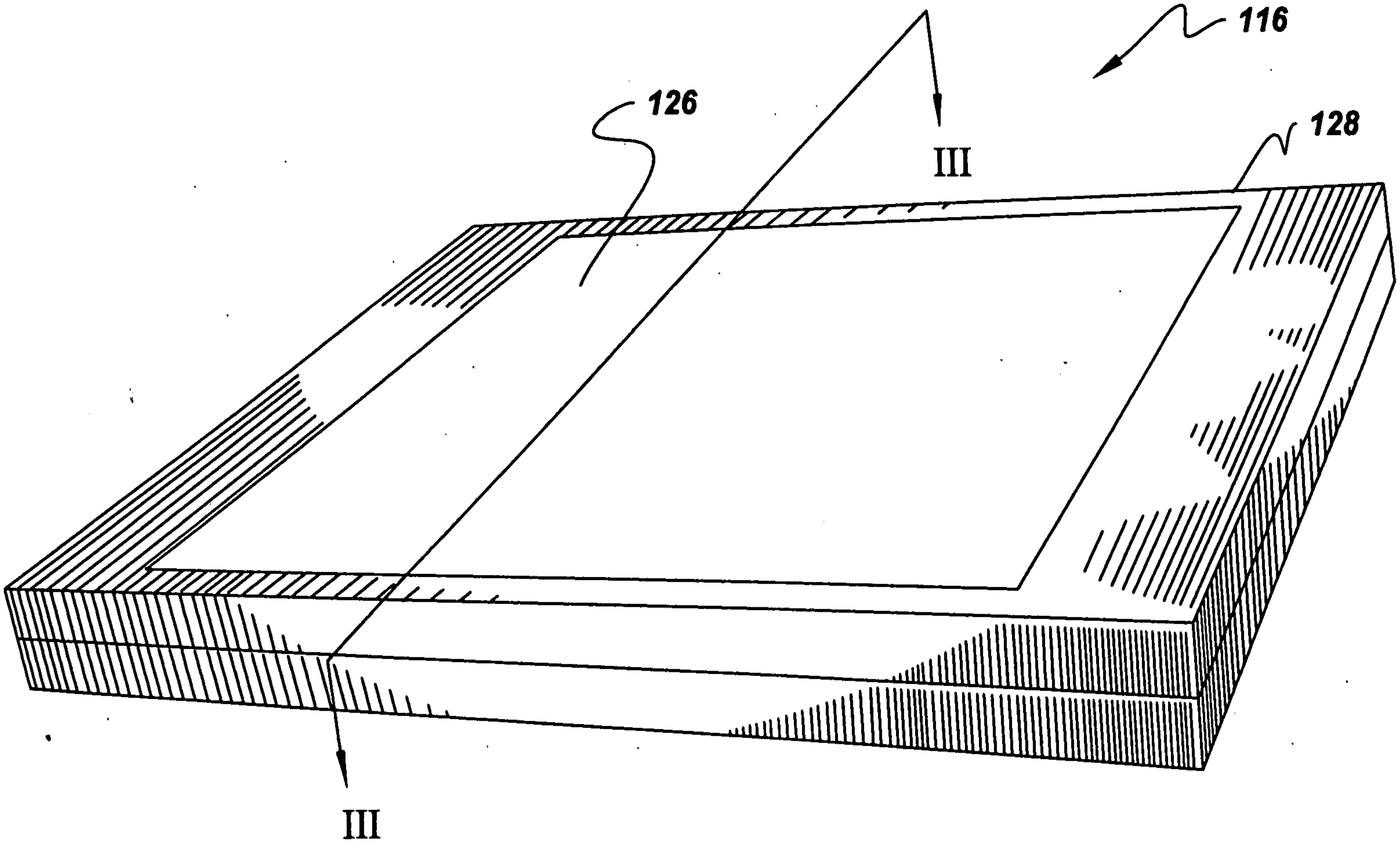


fig. 2
(PRIOR ART)

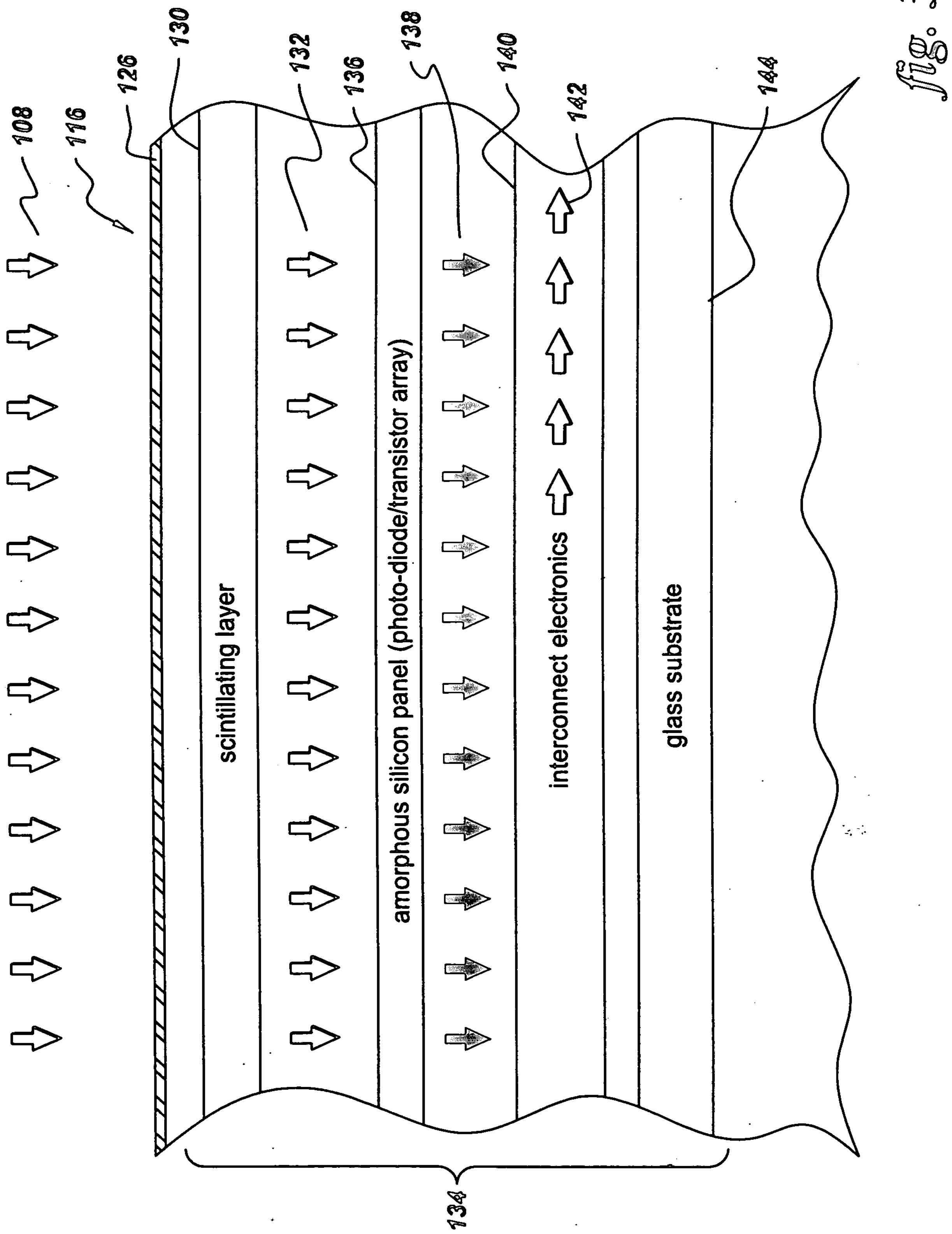

108
116
126
130
132
136
138
140
142
144
134
scintillating layer
amorphous silicon panel (photo-diode/transistor array)
interconnect electronics
glass substrate

fig. 3

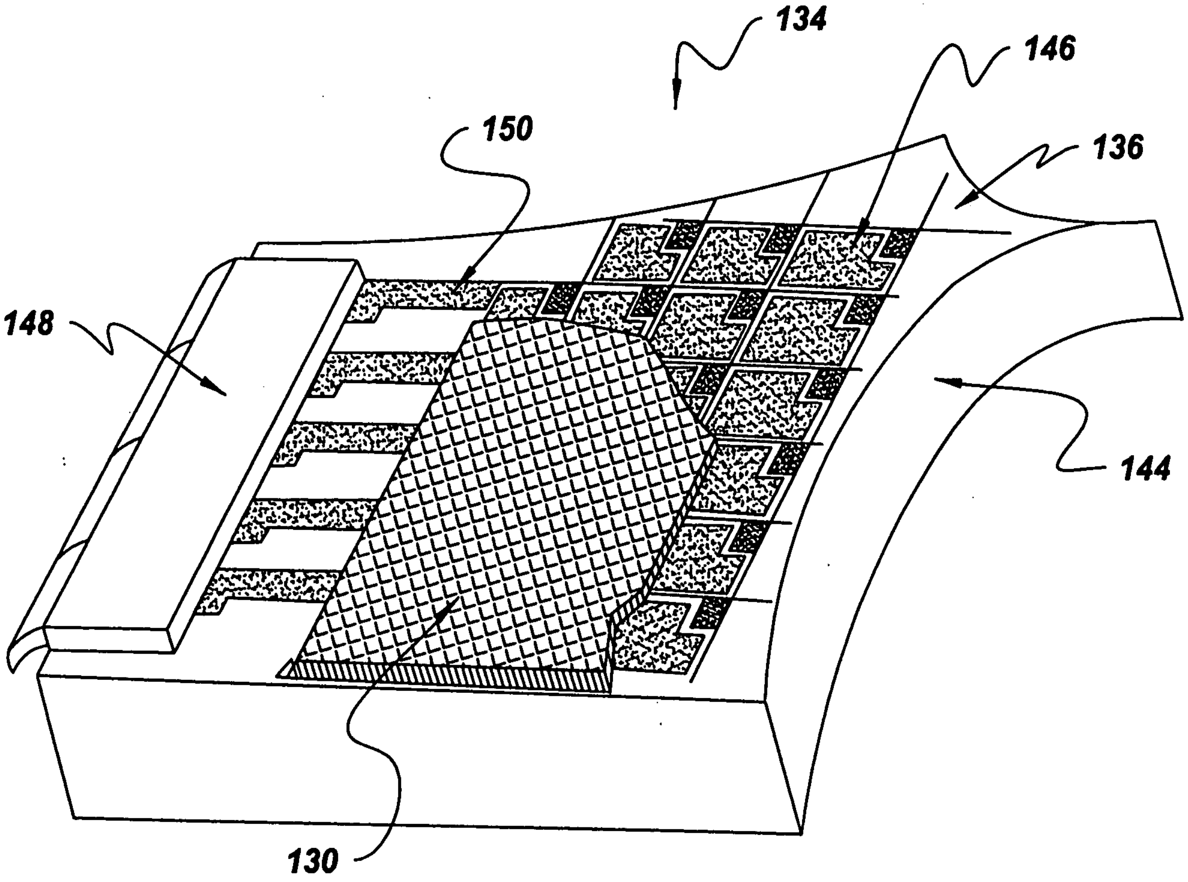


fig. 4
(Prior Art)

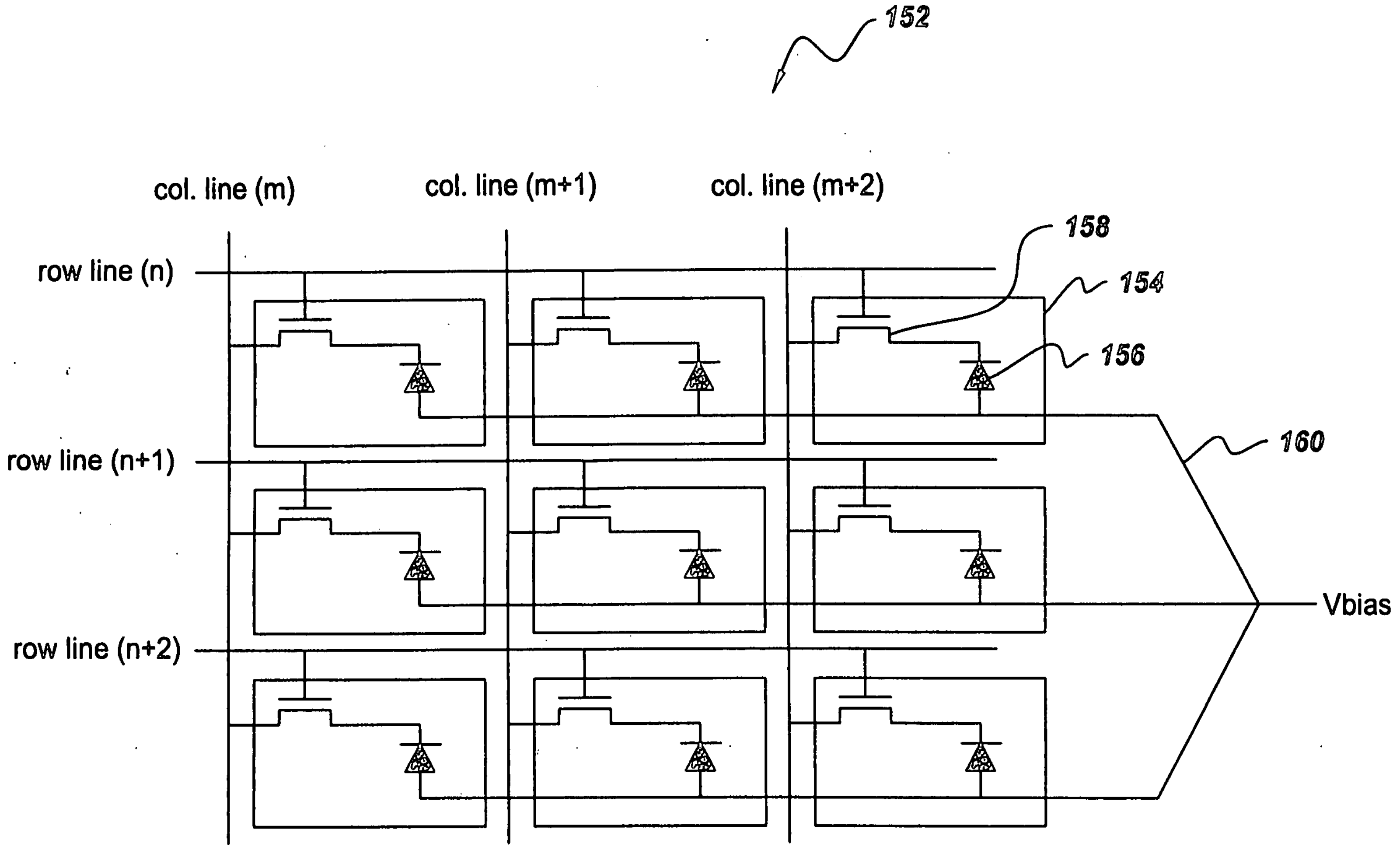


fig. 5
(Prior Art)

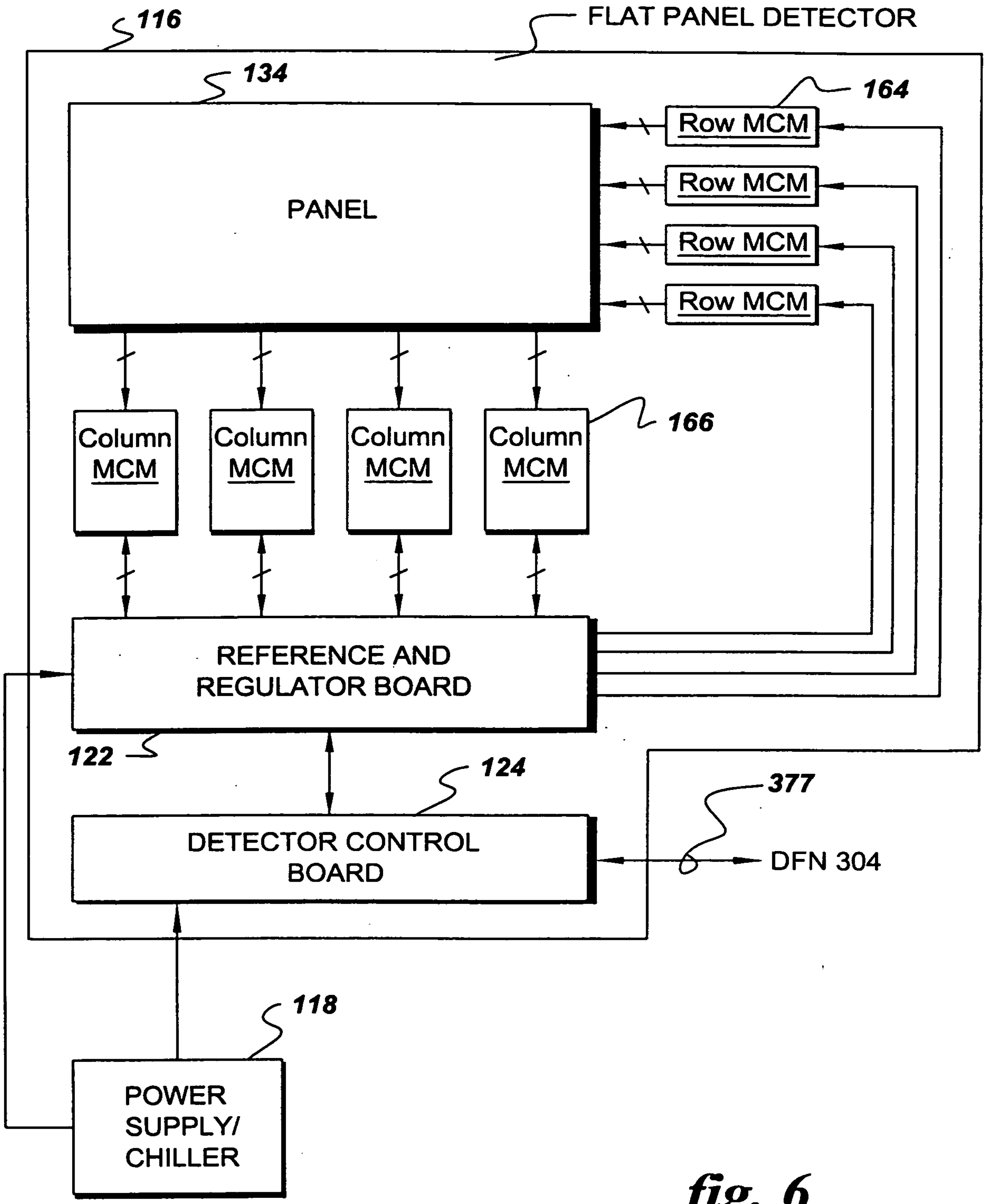


fig. 6
(PRIOR ART)

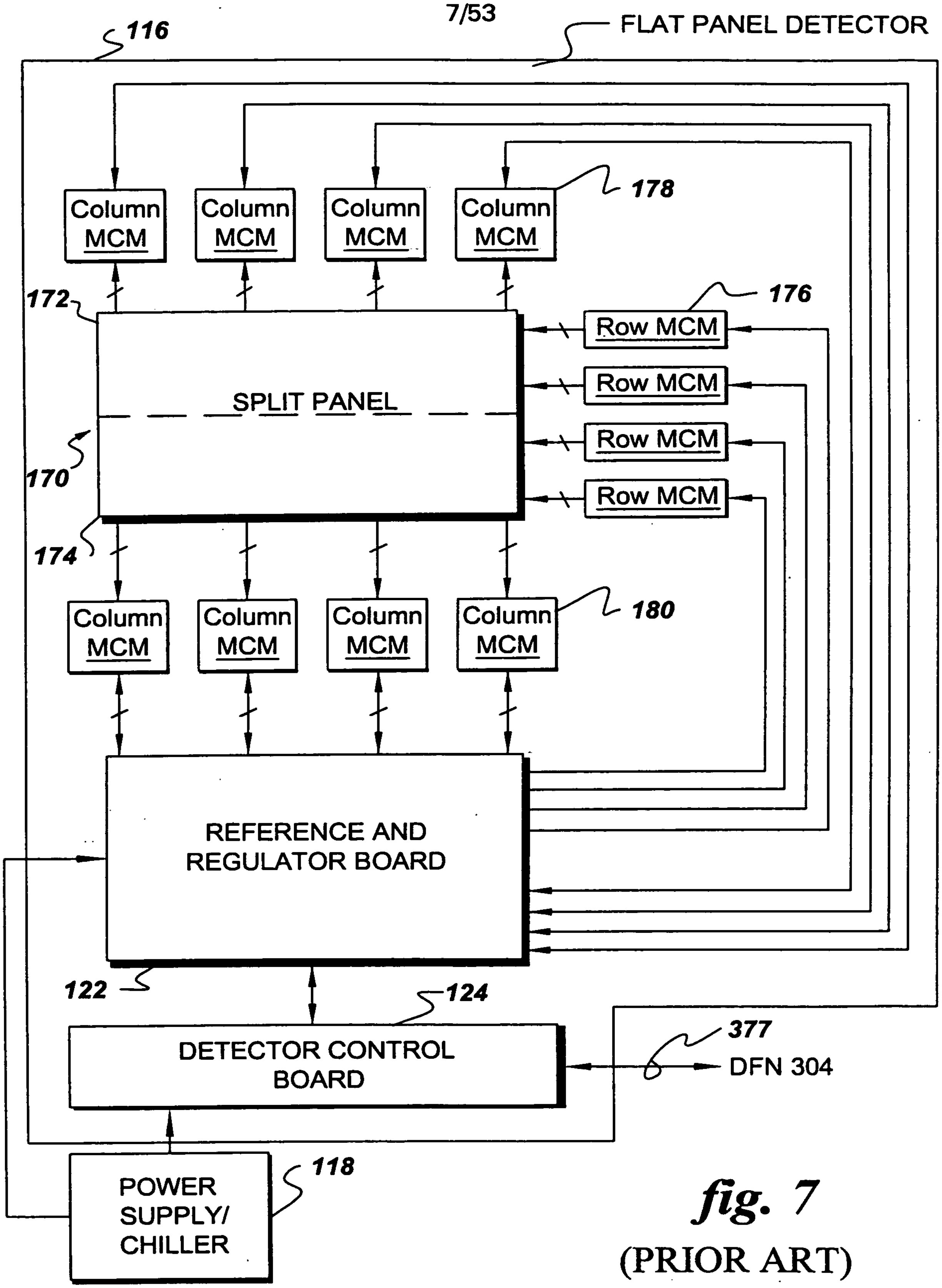
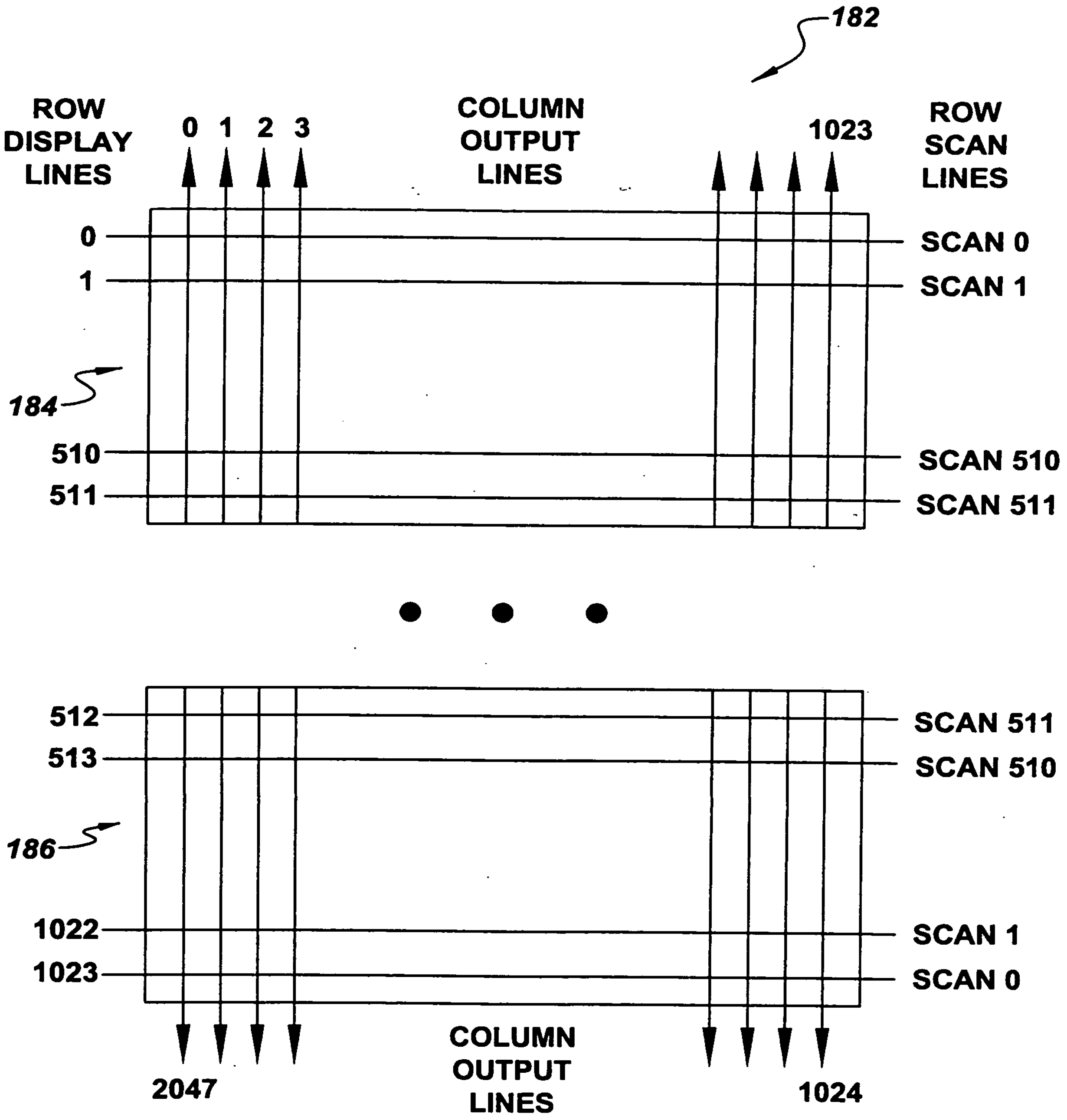


fig. 7
(PRIOR ART)



CARDIAC/SURGICAL DIGITAL X-RAY PANEL

fig. 8
(PRIOR ART)

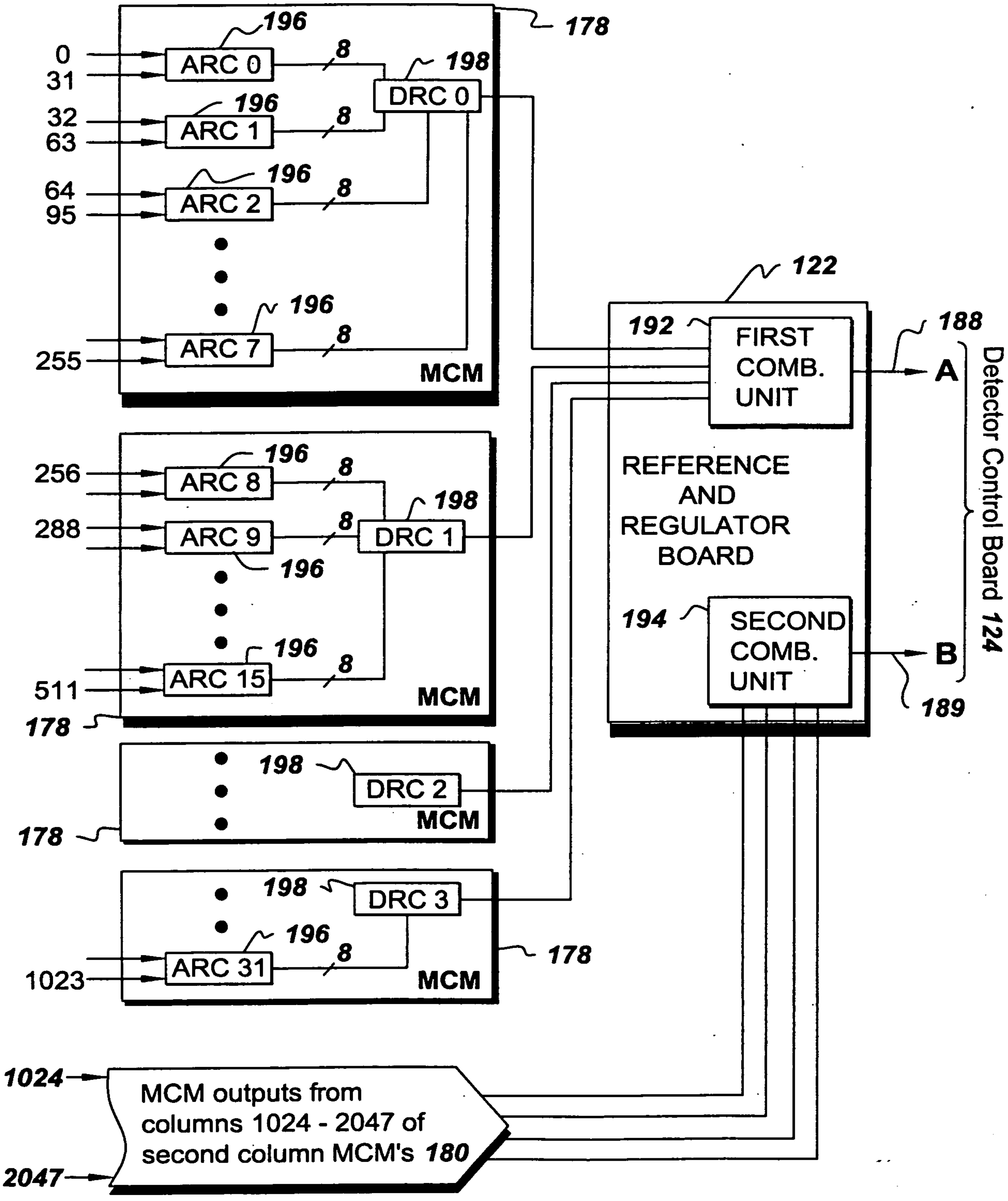


fig. 9 (PRIOR ART)

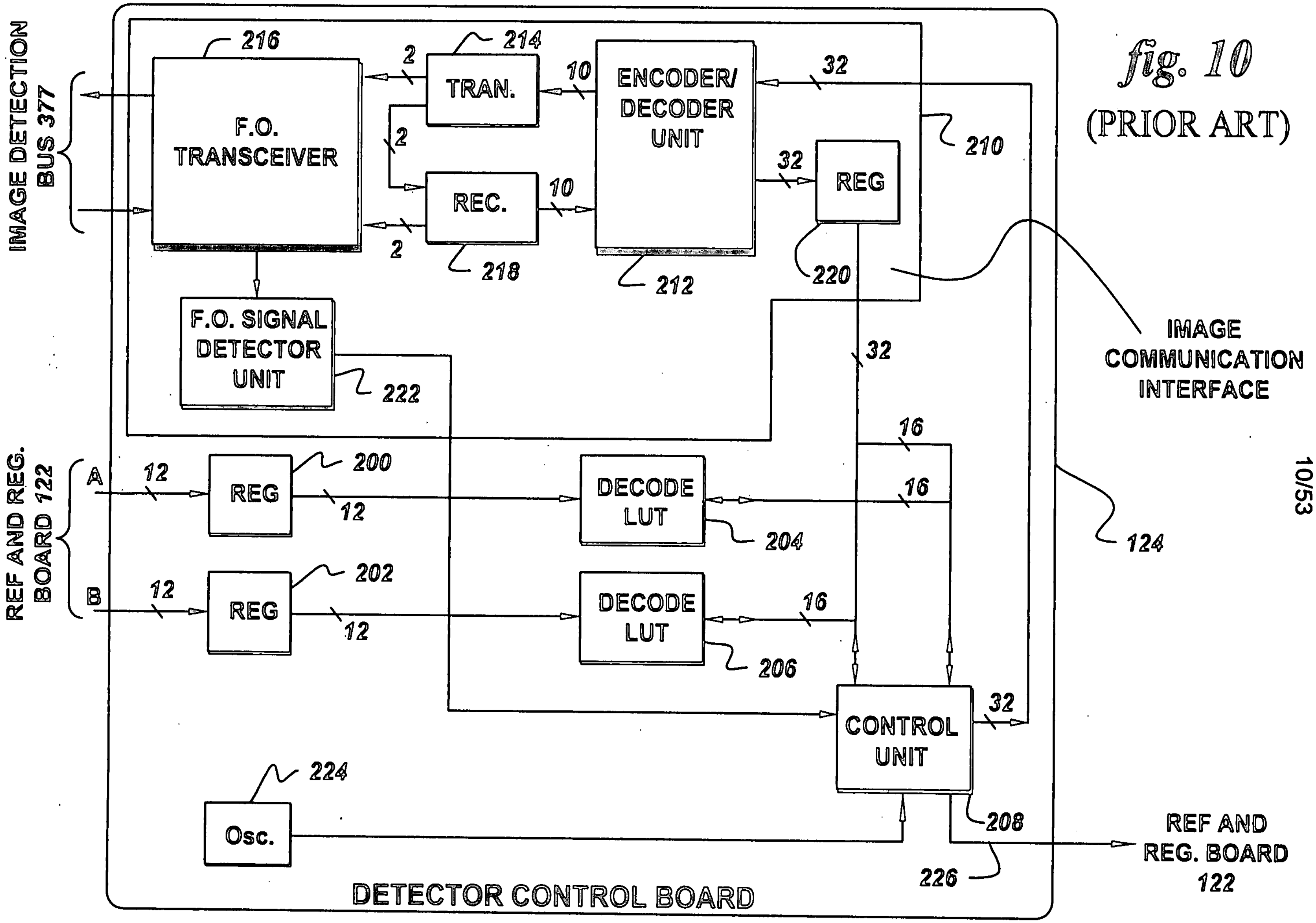
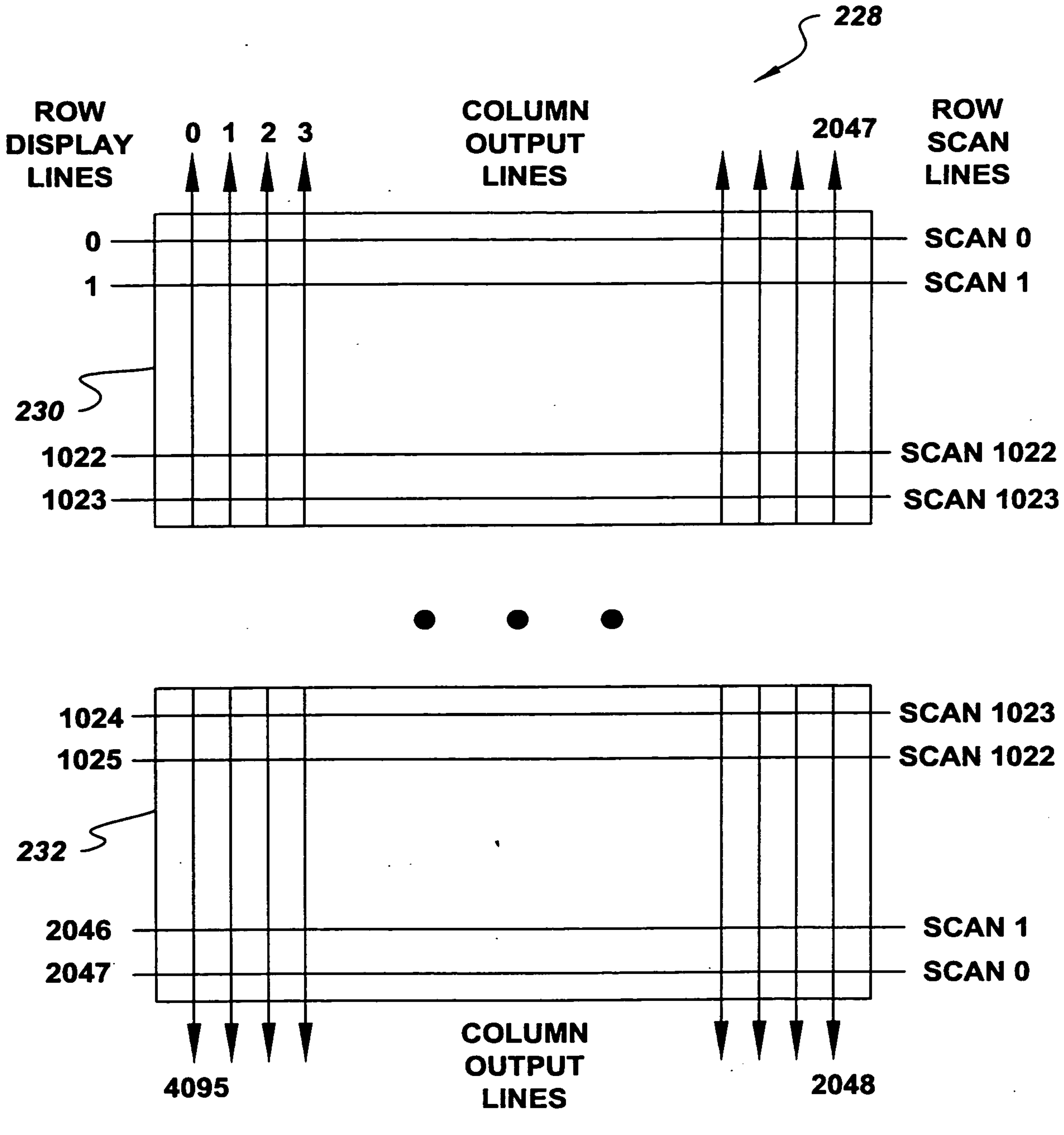


fig. 10
(PRIOR ART)



RADIOGRAPHY DIGITAL X-RAY PANEL

fig. 11 (PRIOR ART)

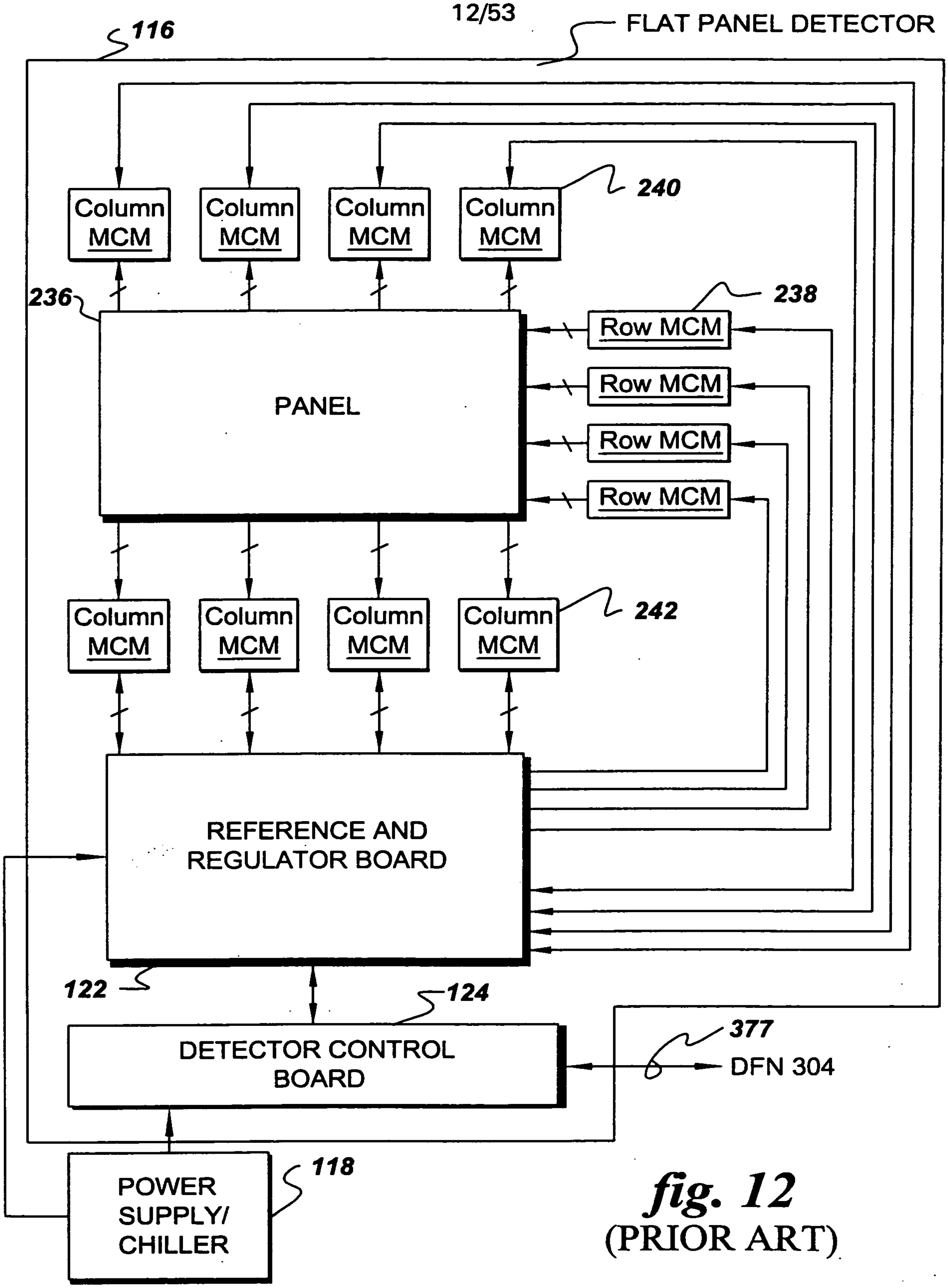
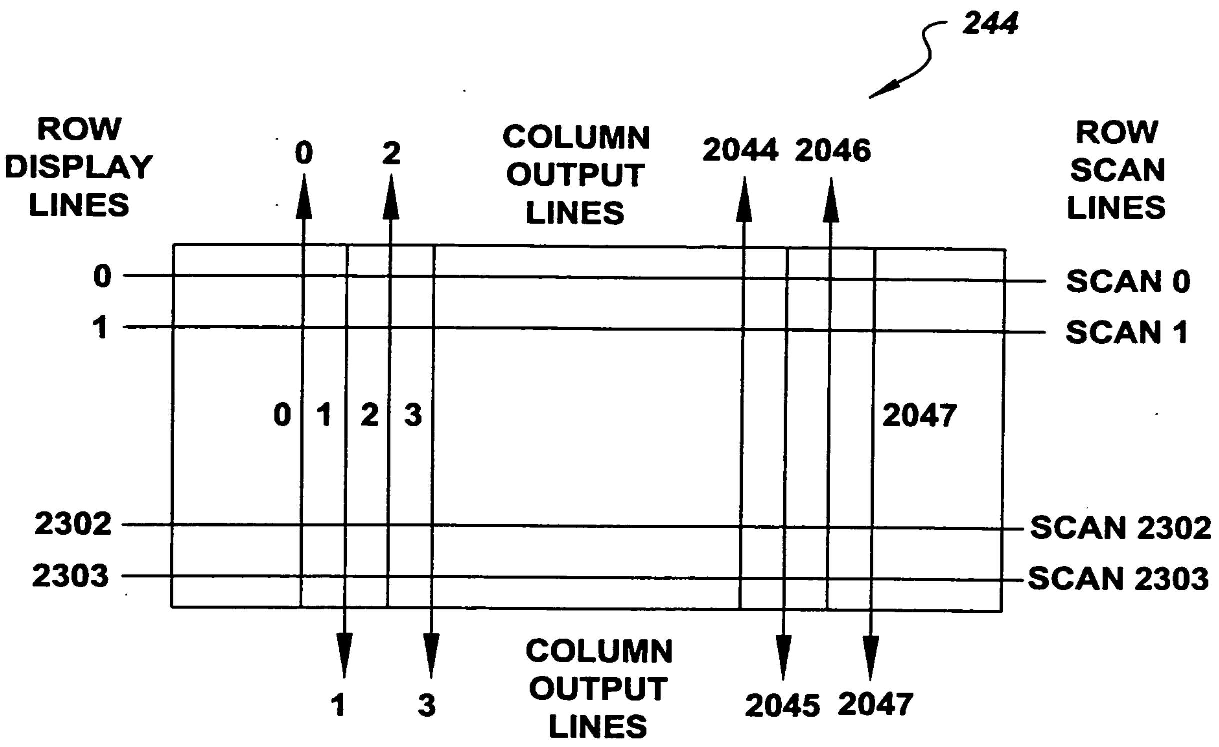


fig. 12
(PRIOR ART)



MAMMOGRAPHY DIGITAL X-RAY PANEL

fig. 13

(PRIOR ART)

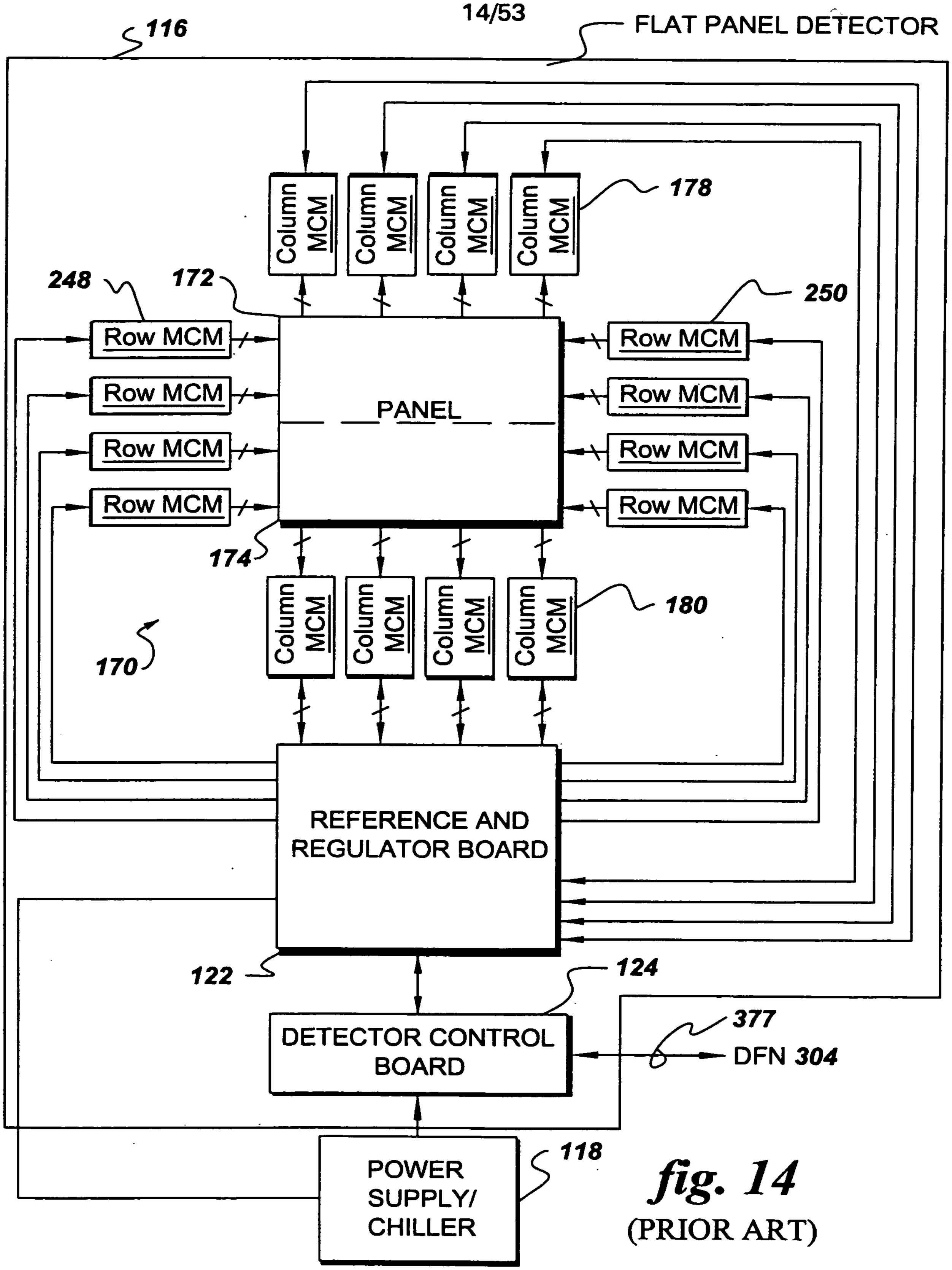


fig. 14
(PRIOR ART)

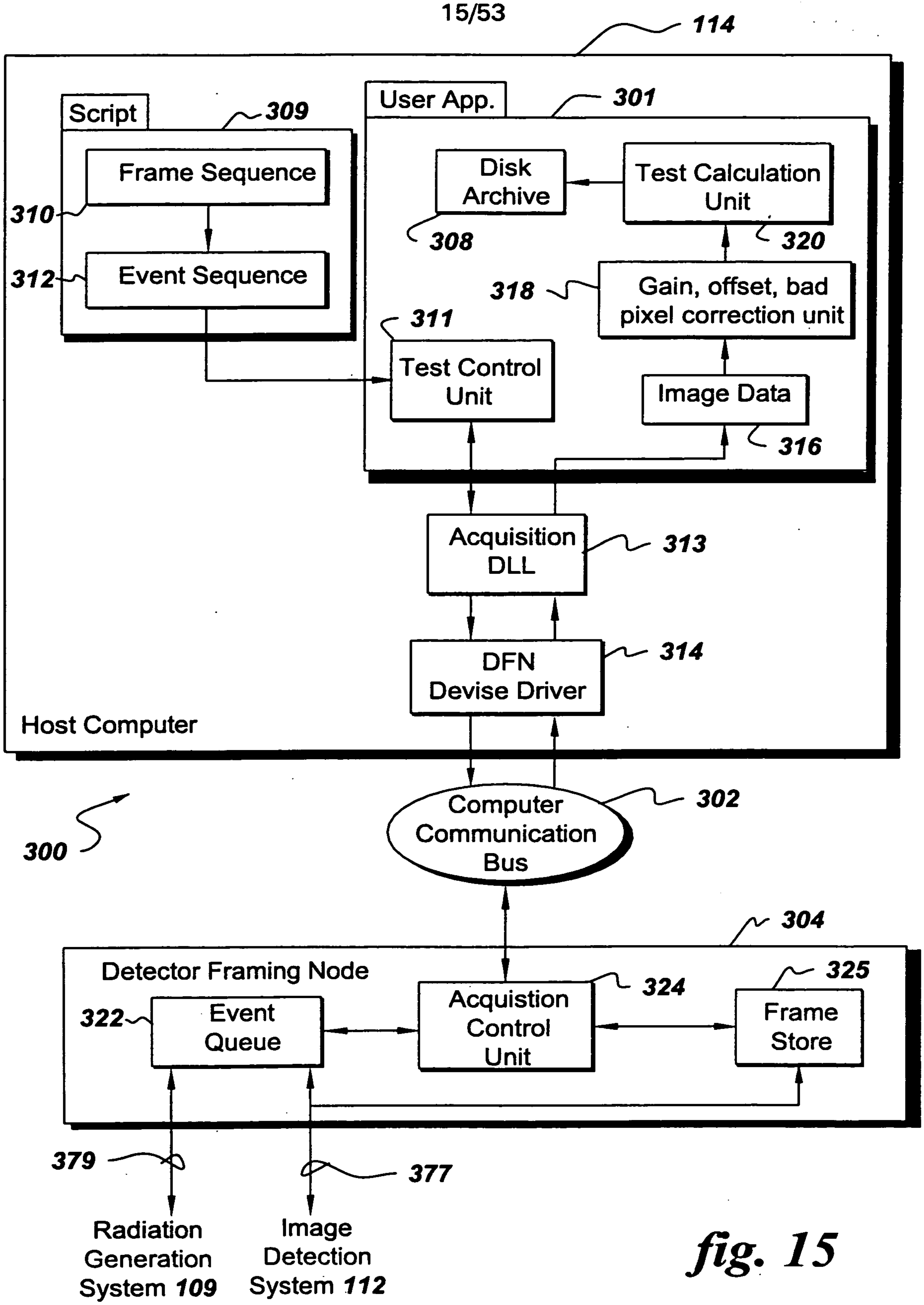

114
Script
309
Frame Sequence
310
312
Event Sequence
User App.
301
Disk Archive
308
Test Calculation Unit
320
318
Gain, offset, bad pixel correction unit
311
Test Control Unit
Image Data
316
Acquisition DLL
313
DFN Devise Driver
314
Host Computer
Computer Communication Bus
302
300
304
Detector Framing Node
Event Queue
322
Acquistion Control Unit
324
Frame Store
325
379
377
Radiation Generation System 109
Image Detection System 112

fig. 15

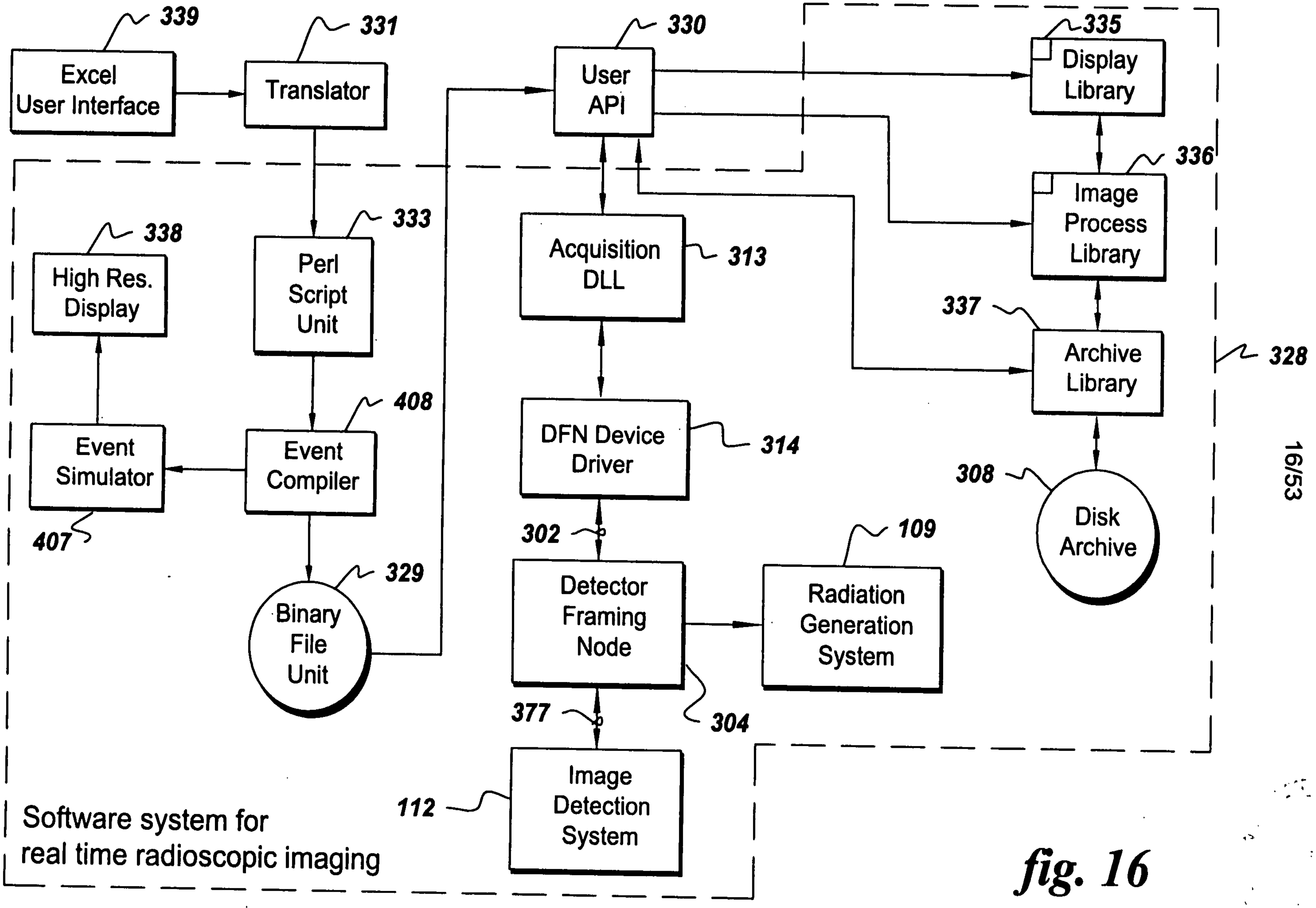

Excel User Interface
339
Translator
331
User API
330
Display Library
335
Image Process Library
336
Archive Library
337
Disk Archive
308
328
High Res. Display
338
Perl Script Unit
333
Event Simulator
407
Event Compiler
408
Binary File Unit
329
Acquisition DLL
313
DFN Device Driver
314
302
Detector Framing Node
304
Radiation Generation System
109
377
Image Detection System
112
Software system for real time radioscopic imaging

fig. 16

fig. 17

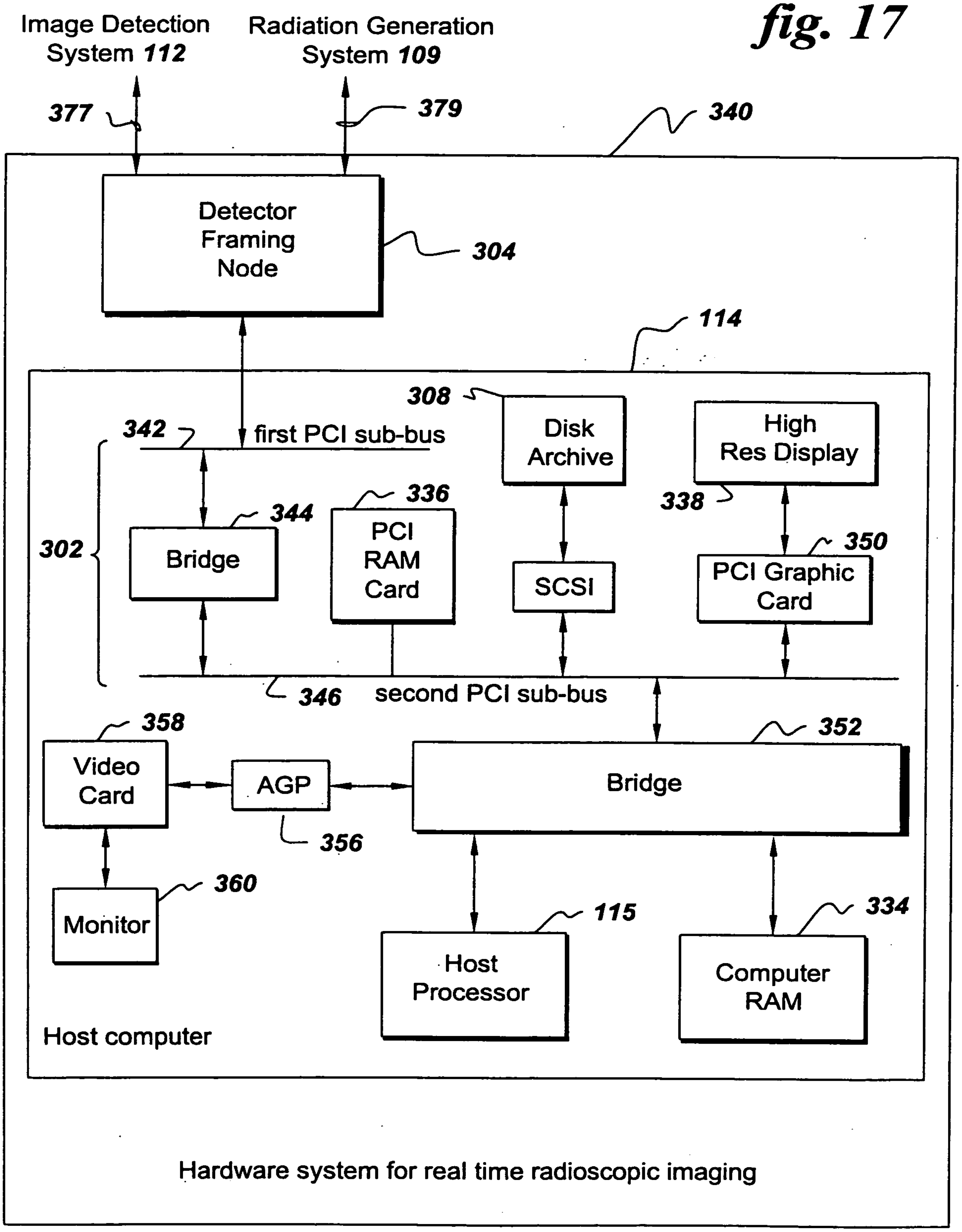


Image Detection System 112
Radiation Generation System 109
377
379
340
Detector Framing Node
304
114
308
Disk Archive
High Res Display
342
first PCI sub-bus
338
336
344
350
302
Bridge
PCI RAM Card
SCSI
PCI Graphic Card
346
second PCI sub-bus
358
352
Video Card
AGP
Bridge
356
360
Monitor
115
334
Host Processor
Computer RAM
Host computer
Hardware system for real time radioscopic imaging

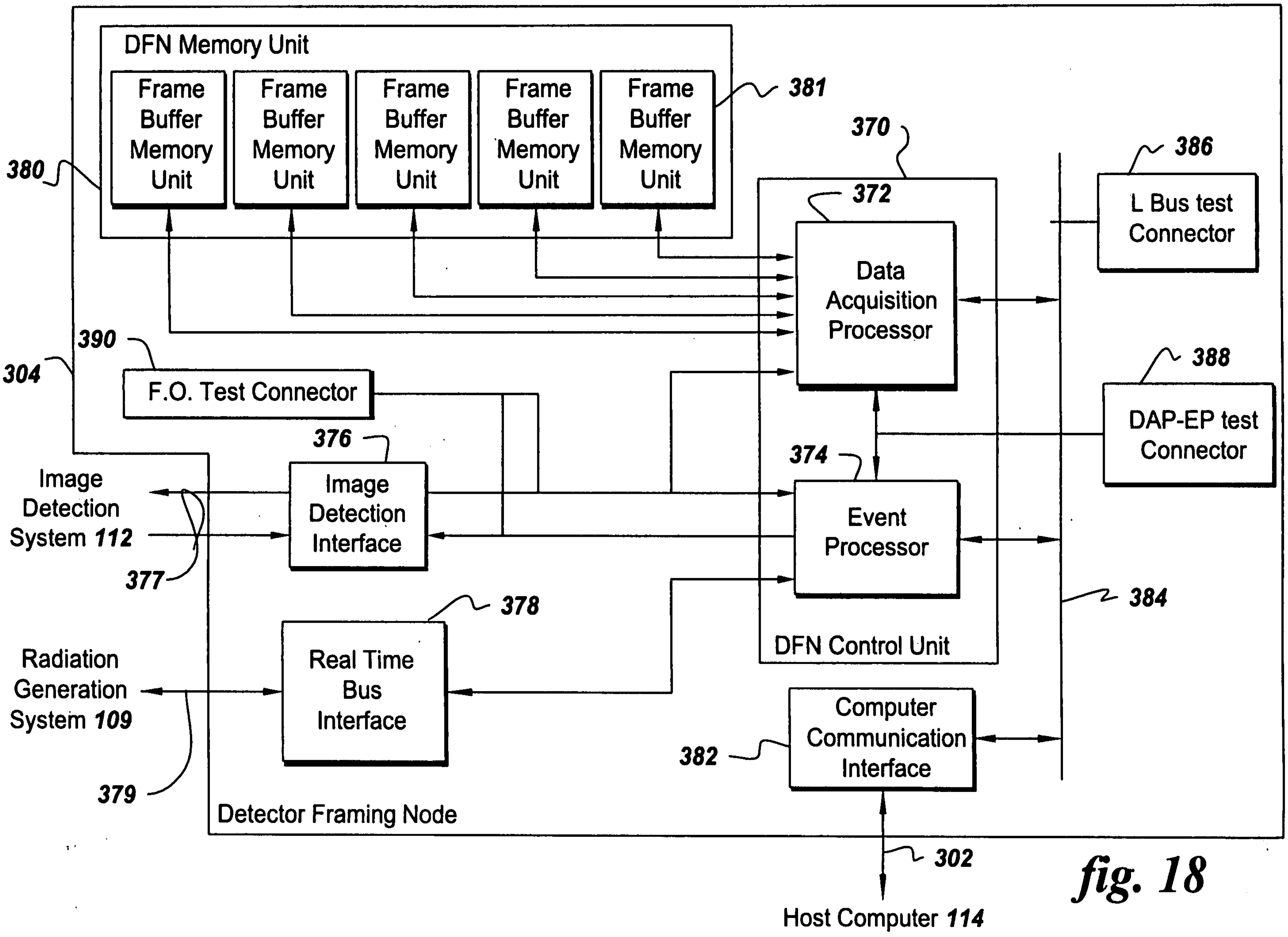

DFN Memory Unit
Frame Buffer Memory Unit
Frame Buffer Memory Unit
Frame Buffer Memory Unit
Frame Buffer Memory Unit
Frame Buffer Memory Unit
381
380
370
372
386
L Bus test Connector
Data Acquisition Processor
390
304
F.O. Test Connector
388
DAP-EP test Connector
376
374
Image Detection System 112
Image Detection Interface
Event Processor
377
378
384
DFN Control Unit
Radiation Generation System 109
Real Time Bus Interface
Computer Communication Interface
382
379
Detector Framing Node
302
Host Computer 114

fig. 18

		(fm/sec)	length	latency	memory	offset	gbr
Panel Setup	Real Time	30	unlimited	<5 frames	host	none	
Single Frame	Post Process	-	-	Delay ~.1 sec	"	y	
Single Frame	Post Process	-	-	Delay ~.2 sec	"	y	y
Real Time	Real Time	R	unlimited	<5 frames	host	none	
Real Time	Real Time	R-X	unlimited	<5 frames	"	y	
Real Time	Real Time	R-Y	unlimited	<5 frames	"	y	y

fig. 19

Modality	image size	Frames Stored host memory
Cardiac	1024 X 1024	200
Rad	2048 X 2048	50
Mammo	2304 X 2048	44

fig. 20

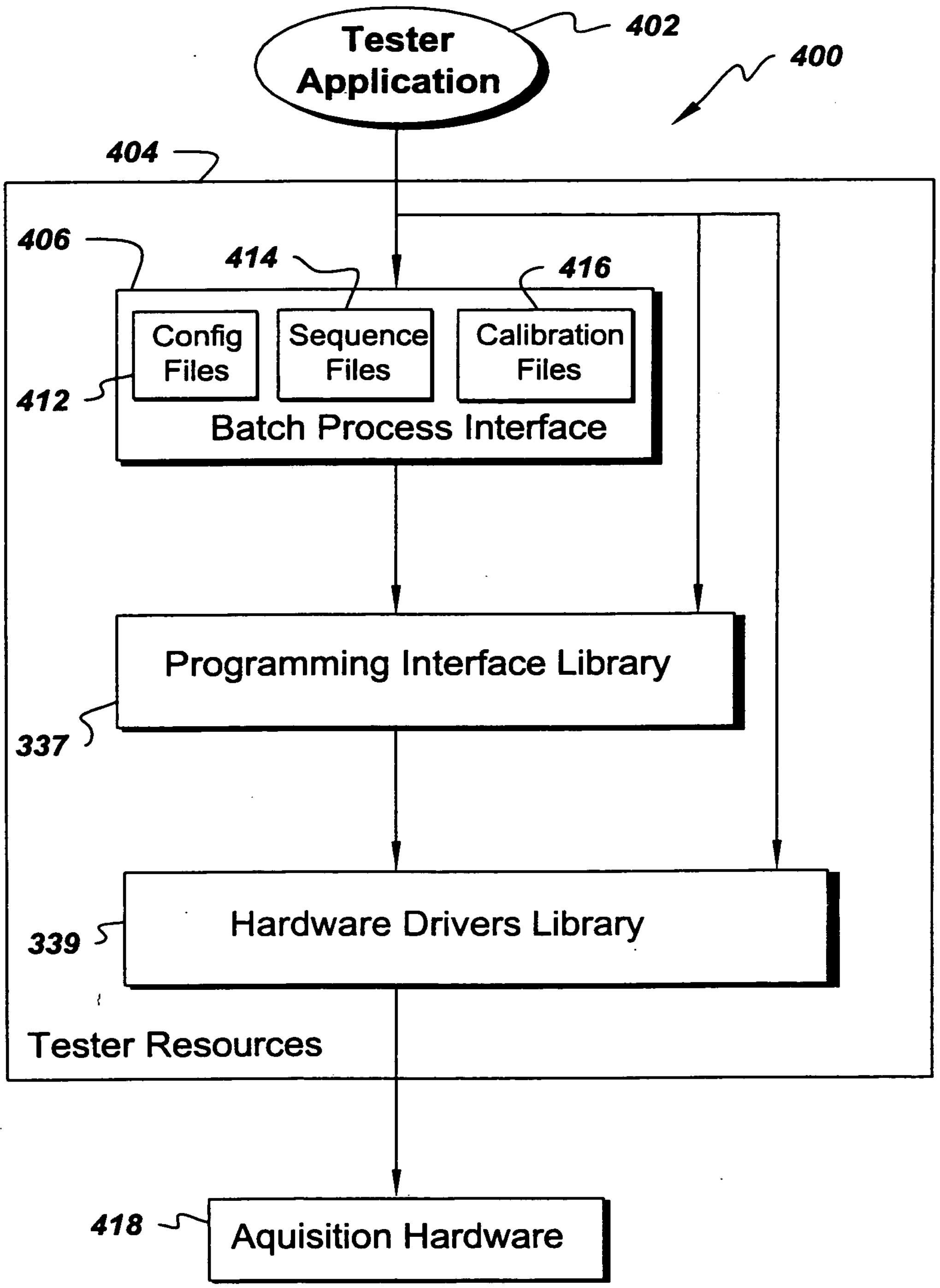

Tester Application
402
400
404
406
414
416
Config Files
Sequence Files
Calibration Files
412
Batch Process Interface
Programming Interface Library
337
Hardware Drivers Library
339
Tester Resources
418
Aquisition Hardware

fig. 21

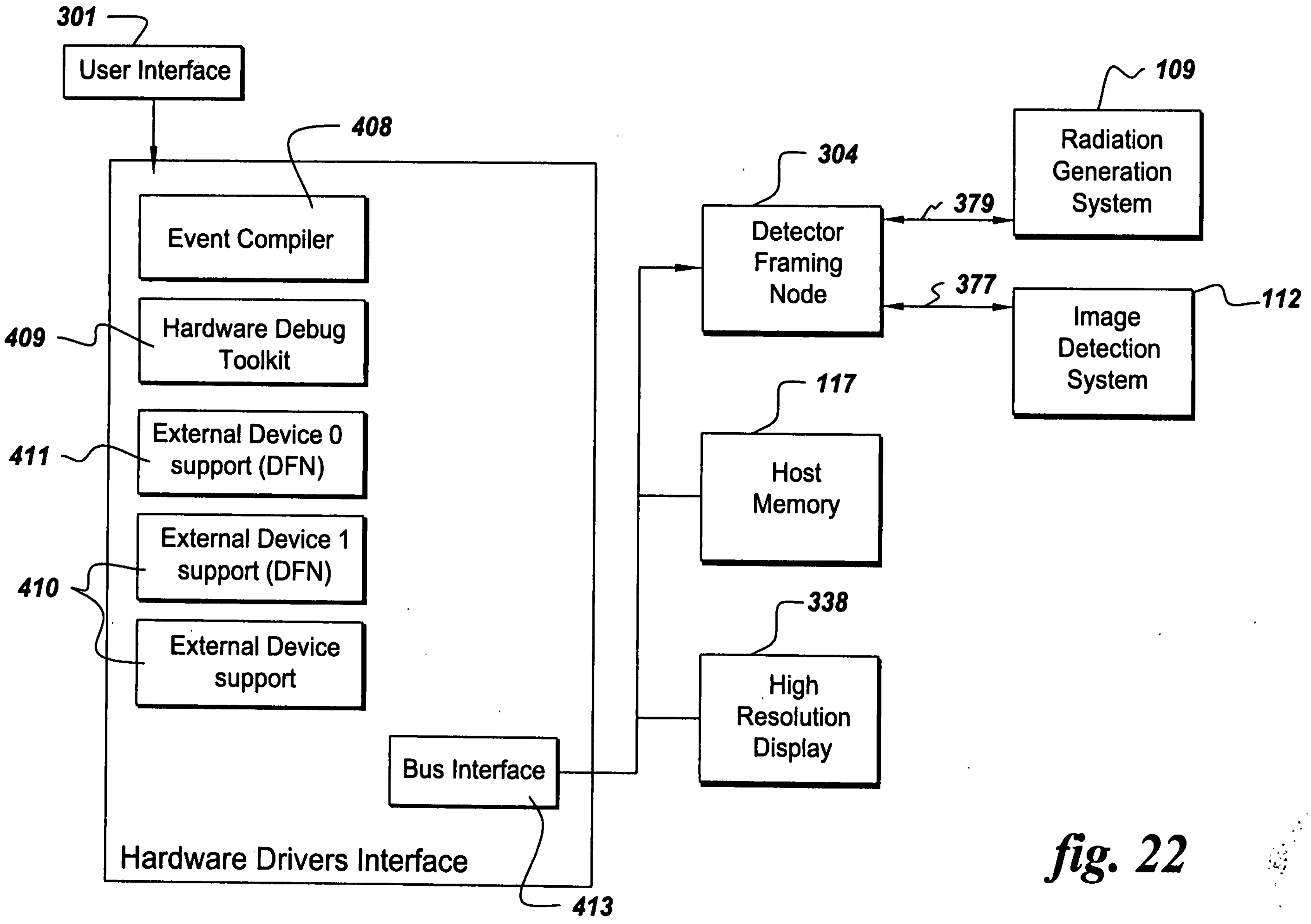

301
User Interface
408
Event Compiler
409
Hardware Debug Toolkit
411
External Device 0 support (DFN)
410
External Device 1 support (DFN)
External Device support
Bus Interface
413
Hardware Drivers Interface
304
Detector Framing Node
117
Host Memory
338
High Resolution Display
379
377
109
Radiation Generation System
112
Image Detection System

fig. 22

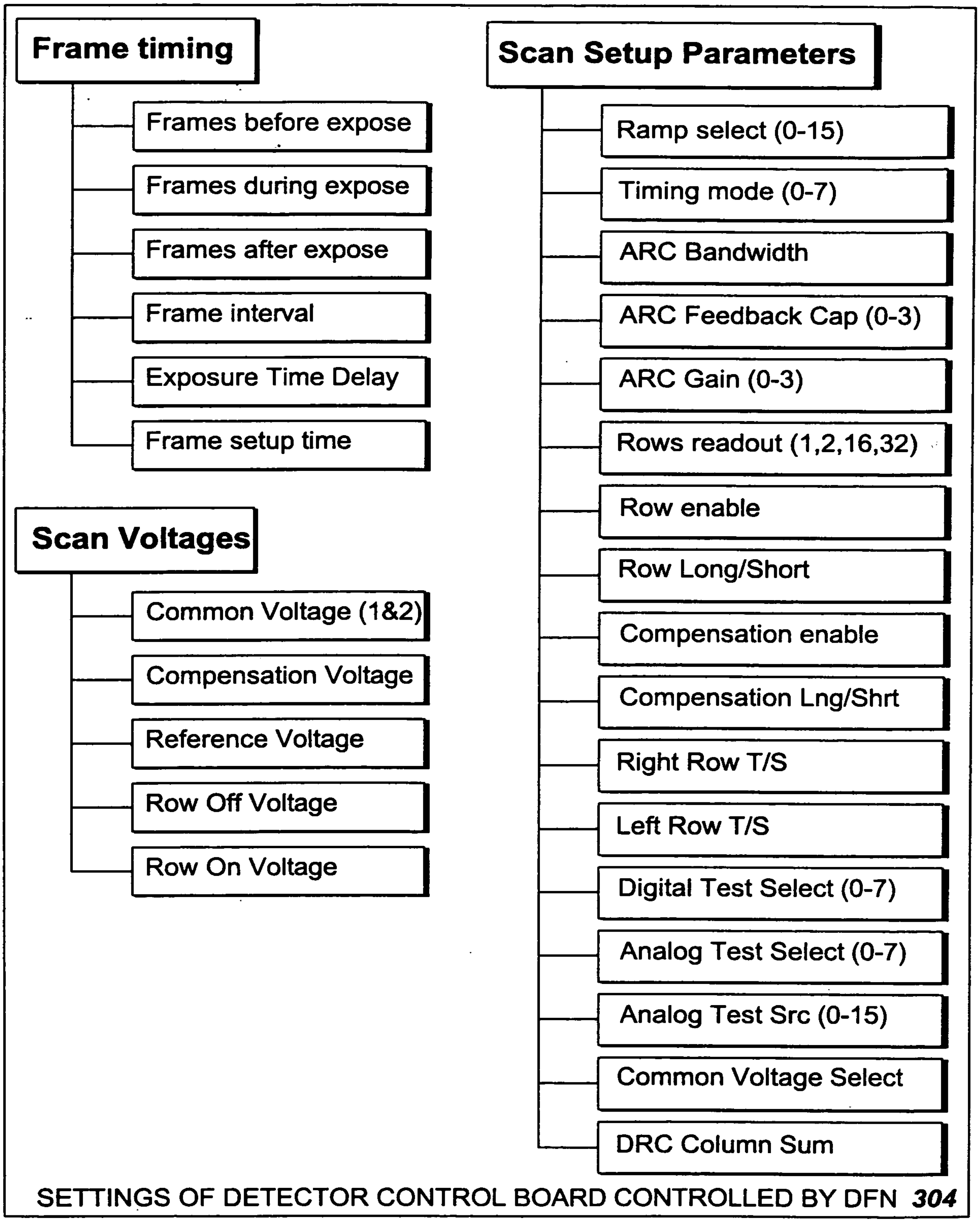

Frame timing
Frames before expose
Frames during expose
Frames after expose
Frame interval
Exposure Time Delay
Frame setup time
Scan Voltages
Common Voltage (1&2)
Compensation Voltage
Reference Voltage
Row Off Voltage
Row On Voltage
Scan Setup Parameters
Ramp select (0-15)
Timing mode (0-7)
ARC Bandwidth
ARC Feedback Cap (0-3)
ARC Gain (0-3)
Rows readout (1,2,16,32)
Row enable
Row Long/Short
Compensation enable
Compensation Lng/Shrt
Right Row T/S
Left Row T/S
Digital Test Select (0-7)
Analog Test Select (0-7)
Analog Test Src (0-15)
Common Voltage Select
DRC Column Sum
SETTINGS OF DETECTOR CONTROL BOARD CONTROLLED BY DFN 304

fig. 23

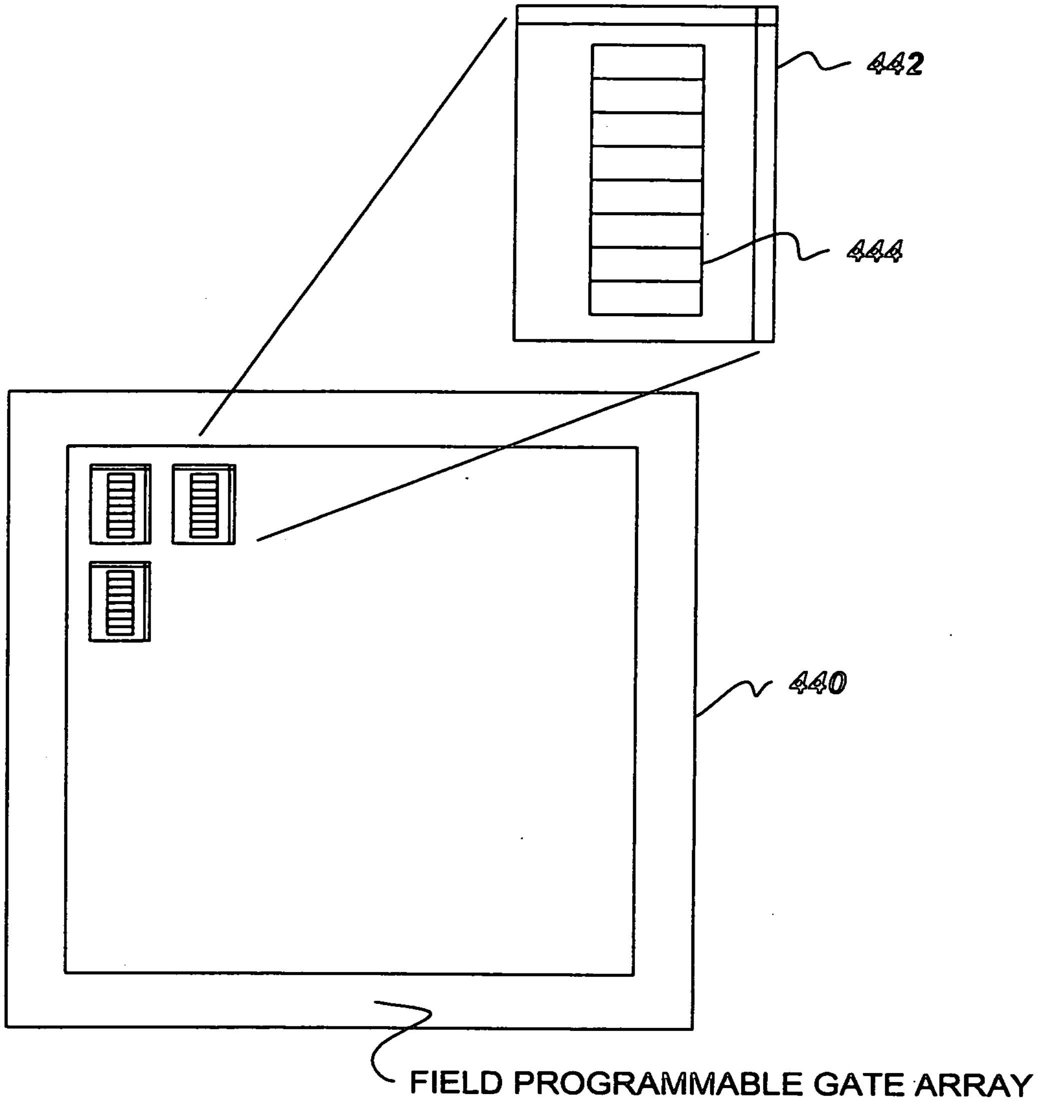


fig. 24

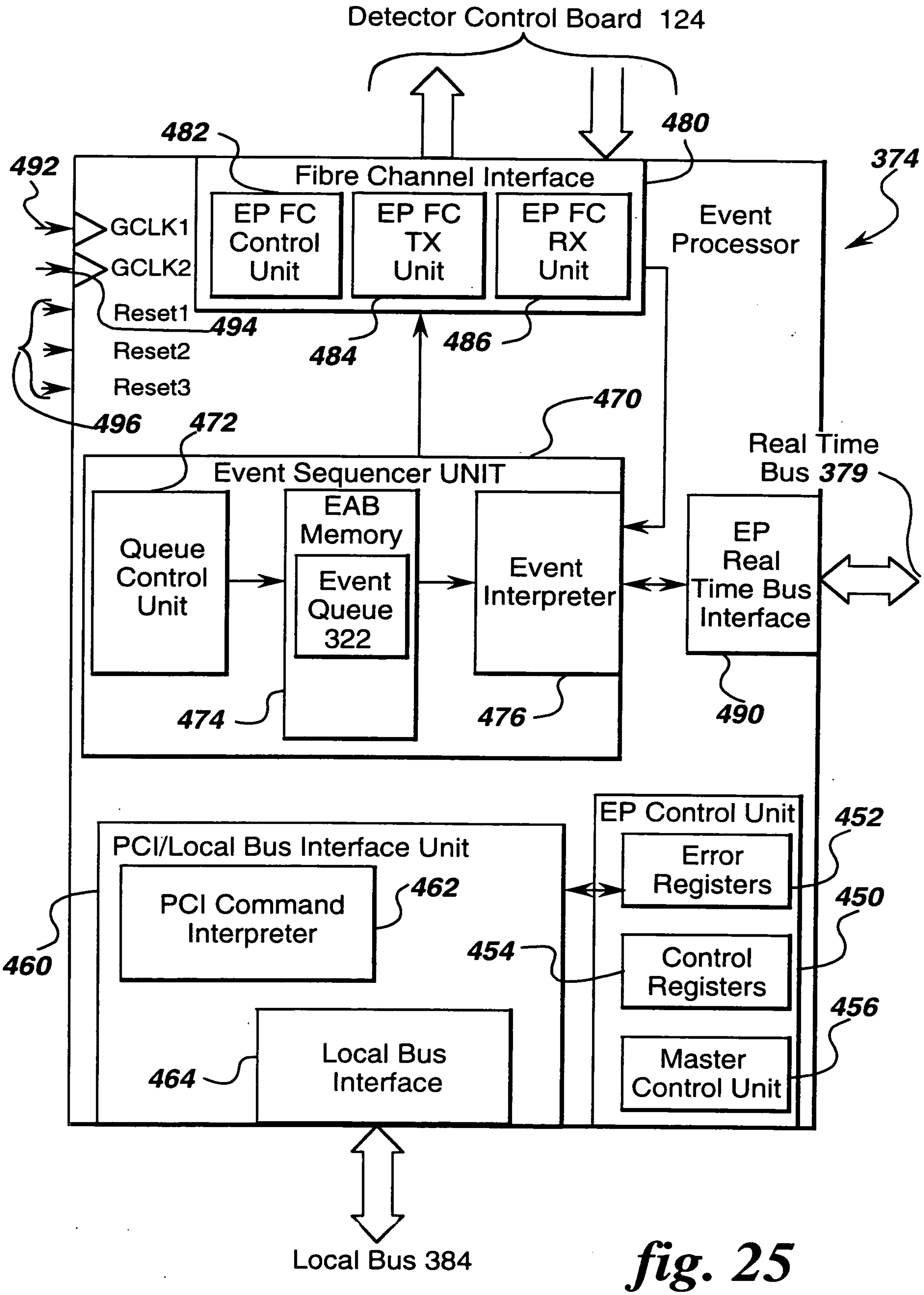

Detector Control Board 124
480
482
374
492
Fibre Channel Interface
EP FC Control Unit
EP FC TX Unit
EP FC RX Unit
Event Processor
GCLK1
GCLK2
Reset1
494
Reset2
Reset3
484
486
496
472
470
Event Sequencer UNIT
Real Time Bus 379
Queue Control Unit
EAB Memory
Event Queue 322
Event Interpreter
EP Real Time Bus Interface
474
476
490
EP Control Unit
452
PCI/Local Bus Interface Unit
Error Registers
PCI Command Interpreter
462
450
460
454
Control Registers
456
Local Bus Interface
464
Master Control Unit
Local Bus 384

fig. 25

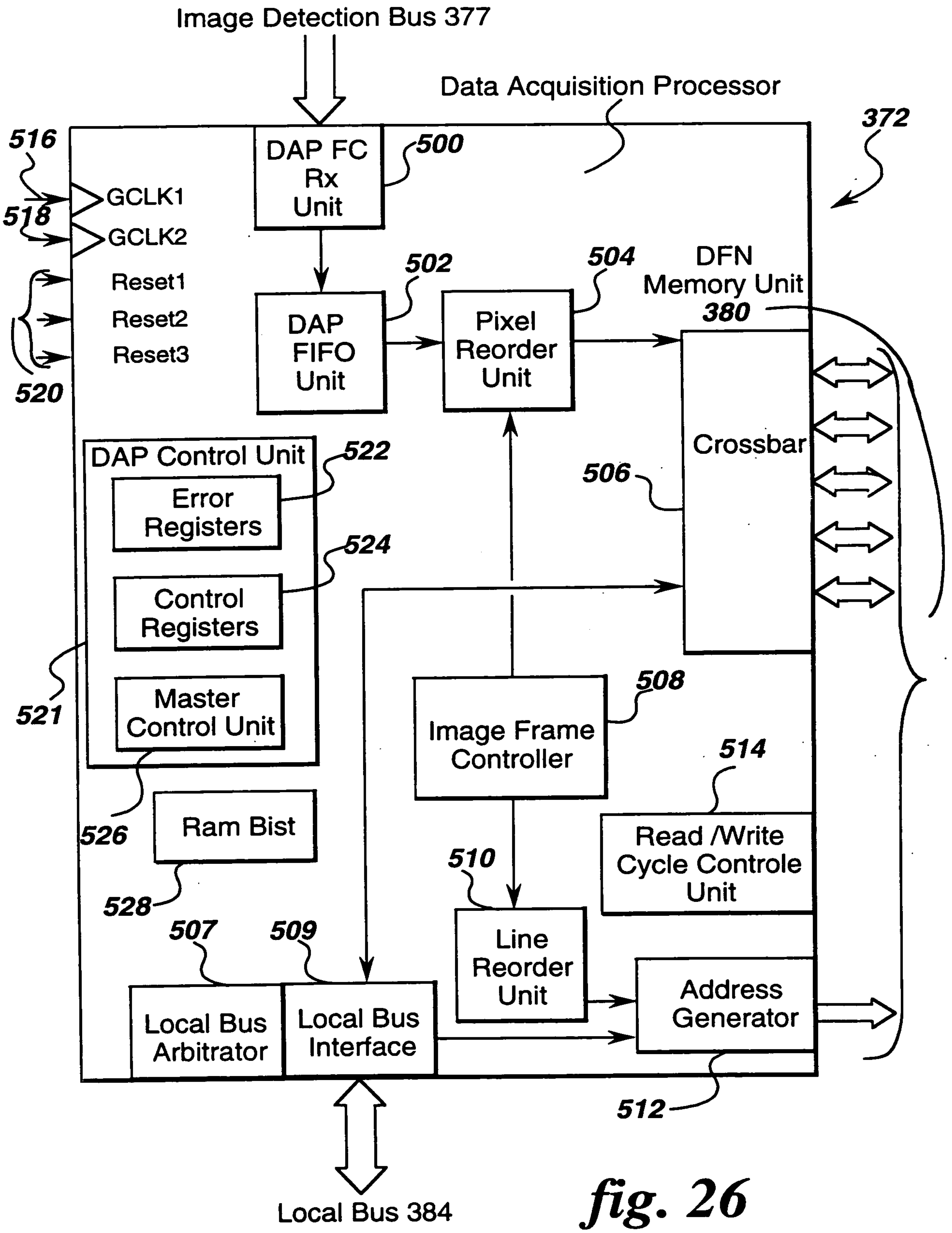


Image Detection Bus 377
Data Acquisition Processor
372
516
GCLK1
518
GCLK2
Reset1
Reset2
Reset3
520
DAP FC Rx Unit
500
DAP FIFO Unit
502
Pixel Reorder Unit
504
DFN Memory Unit 380
Crossbar
506
DAP Control Unit
522
Error Registers
524
Control Registers
521
Master Control Unit
526
Ram Bist
528
Image Frame Controller
508
514
Read /Write Cycle Controle Unit
510
Line Reorder Unit
507
509
Local Bus Arbitrator
Local Bus Interface
Address Generator
512
Local Bus 384

fig. 26

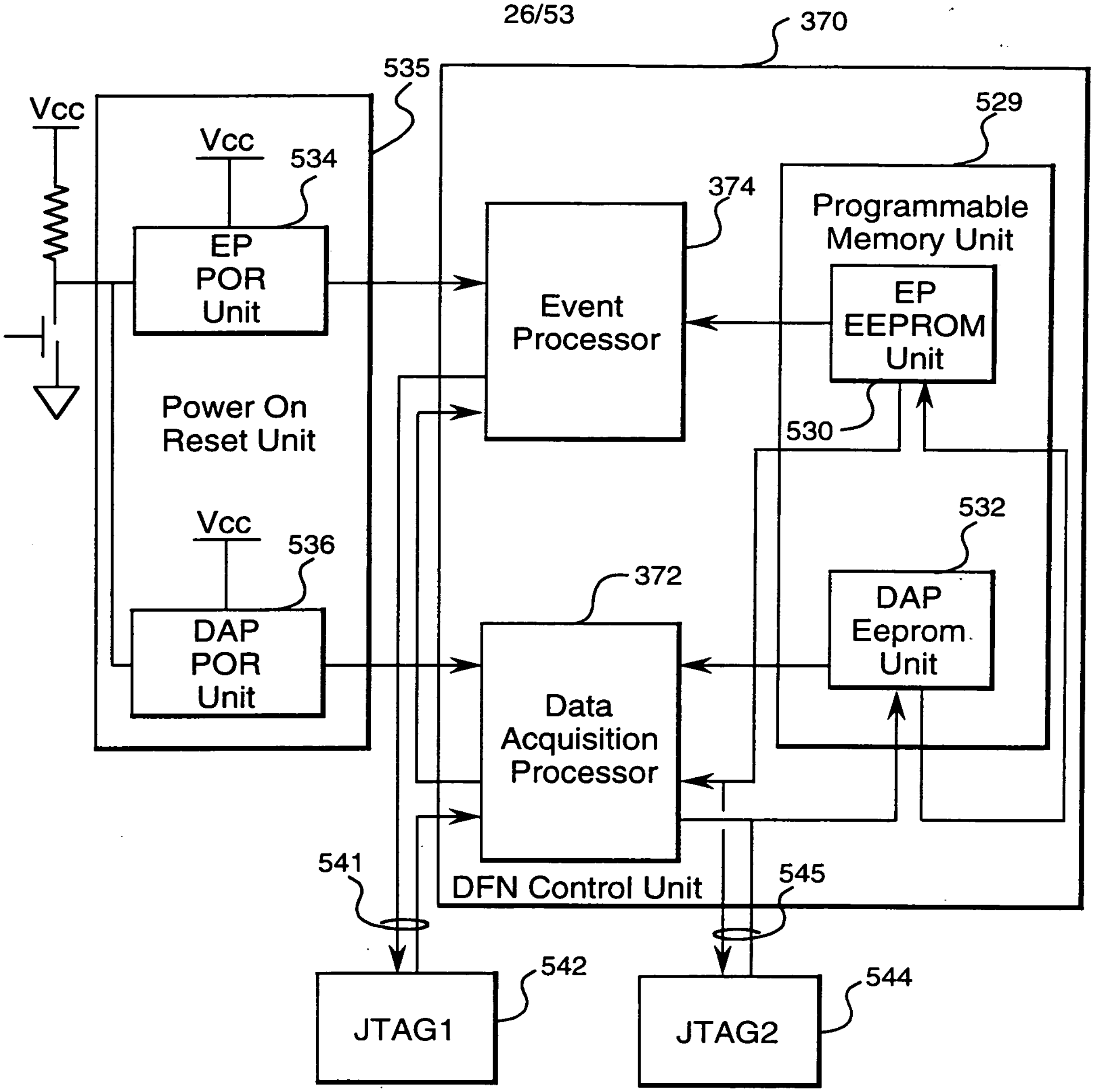

370
535
Vcc
Vcc
534
EP
POR
Unit
Power On
Reset Unit
Vcc
536
DAP
POR
Unit
374
Event
Processor
529
Programmable
Memory Unit
EP
EEPROM
Unit
530
532
DAP
Eeprom
Unit
372
Data
Acquisition
Processor
DFN Control Unit
541
545
542
JTAG1
544
JTAG2

fig. 27

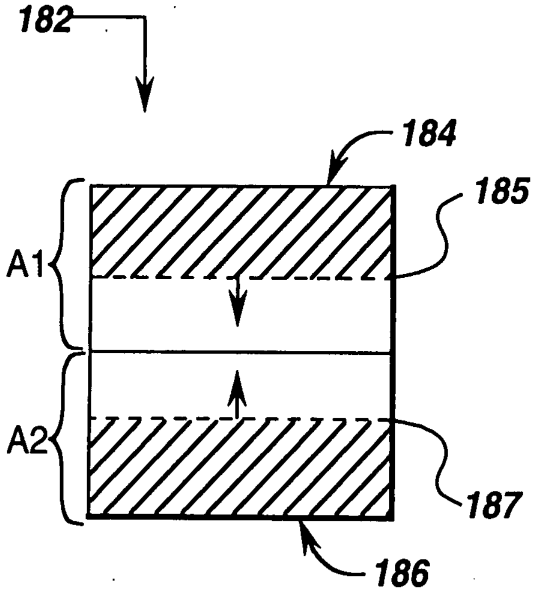


fig. 28

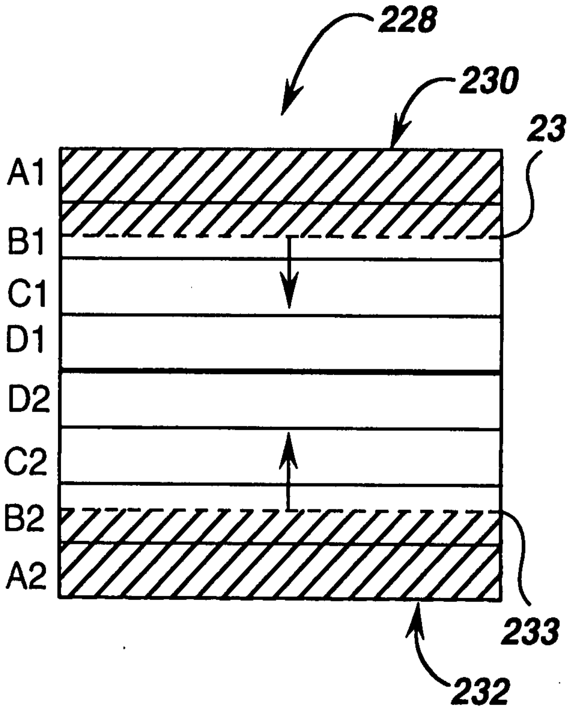


fig. 29

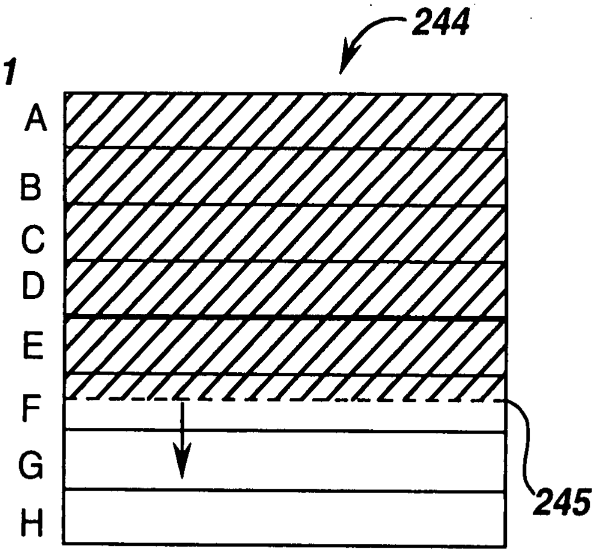


fig. 30

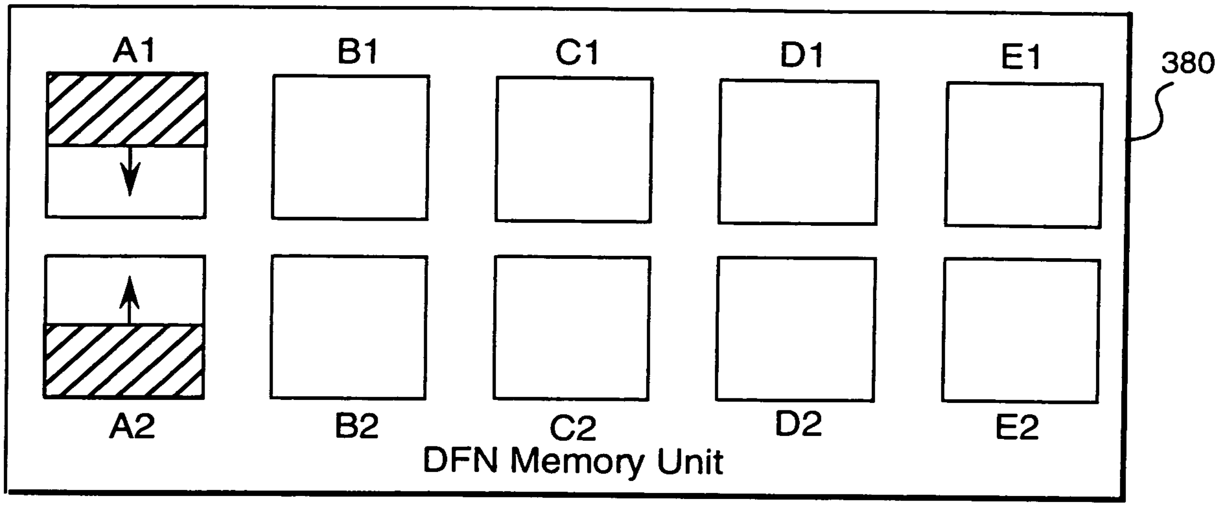


fig. 31

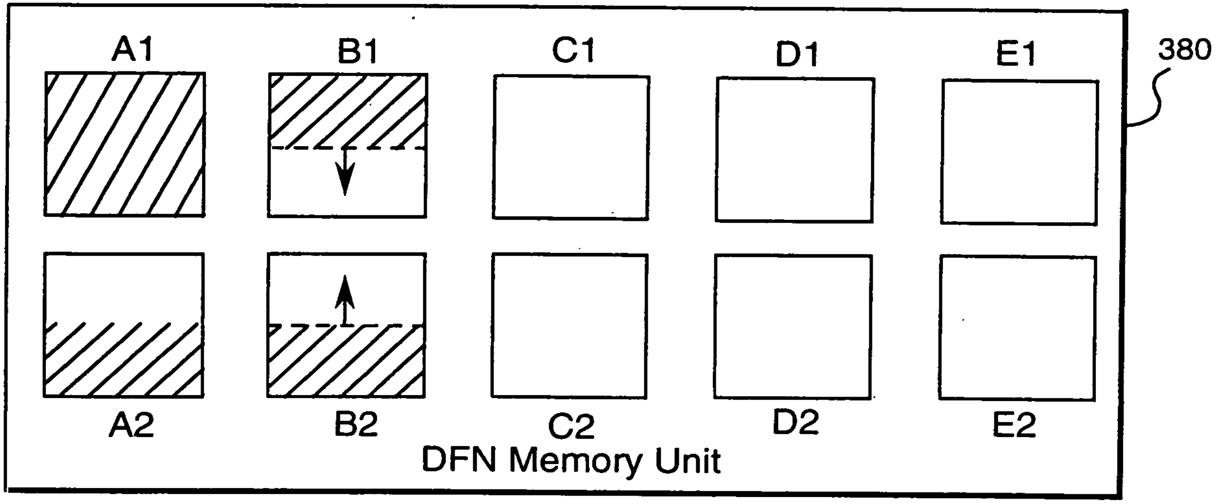


fig. 32

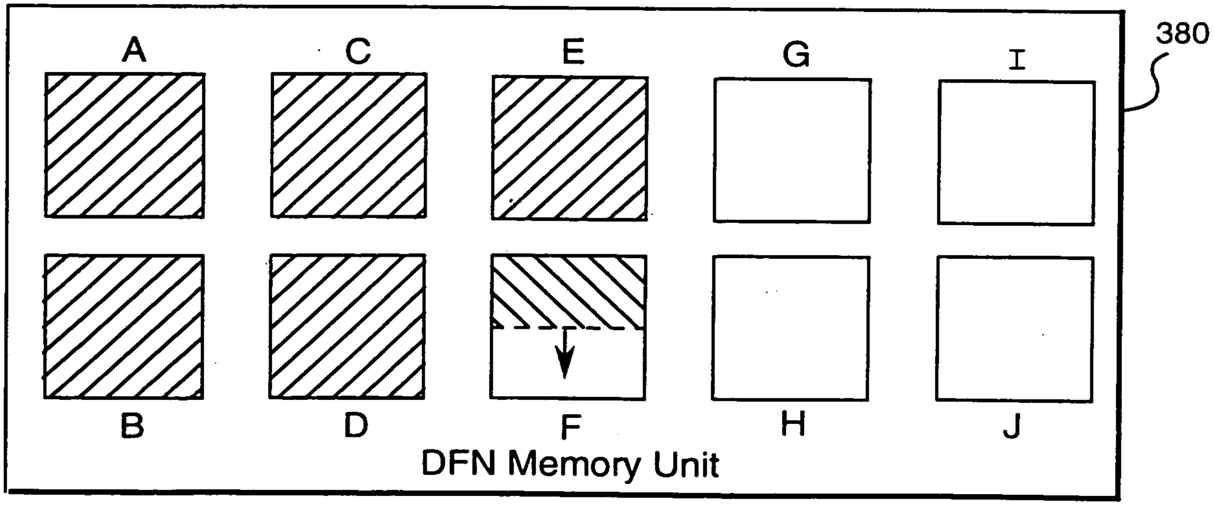


fig. 33

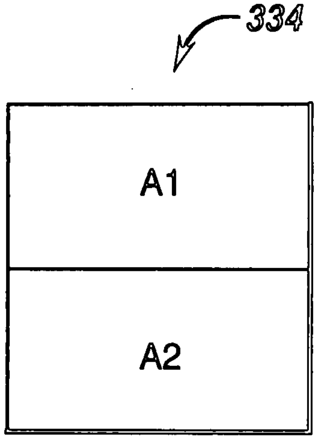


fig. 34

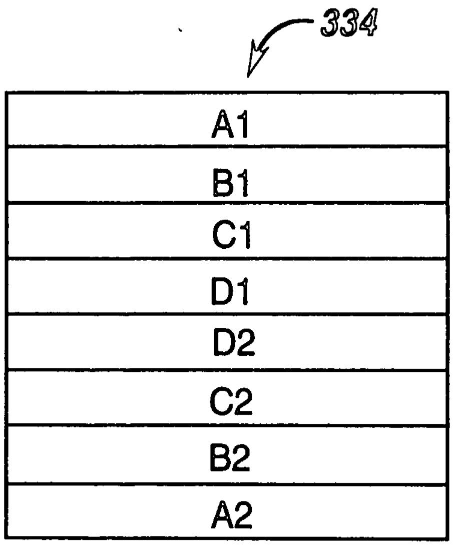


fig. 35

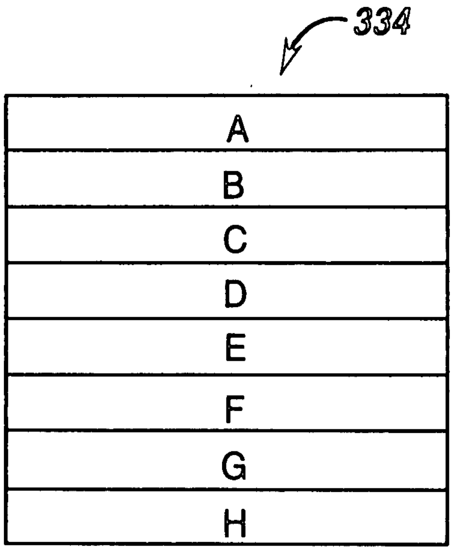


fig. 36

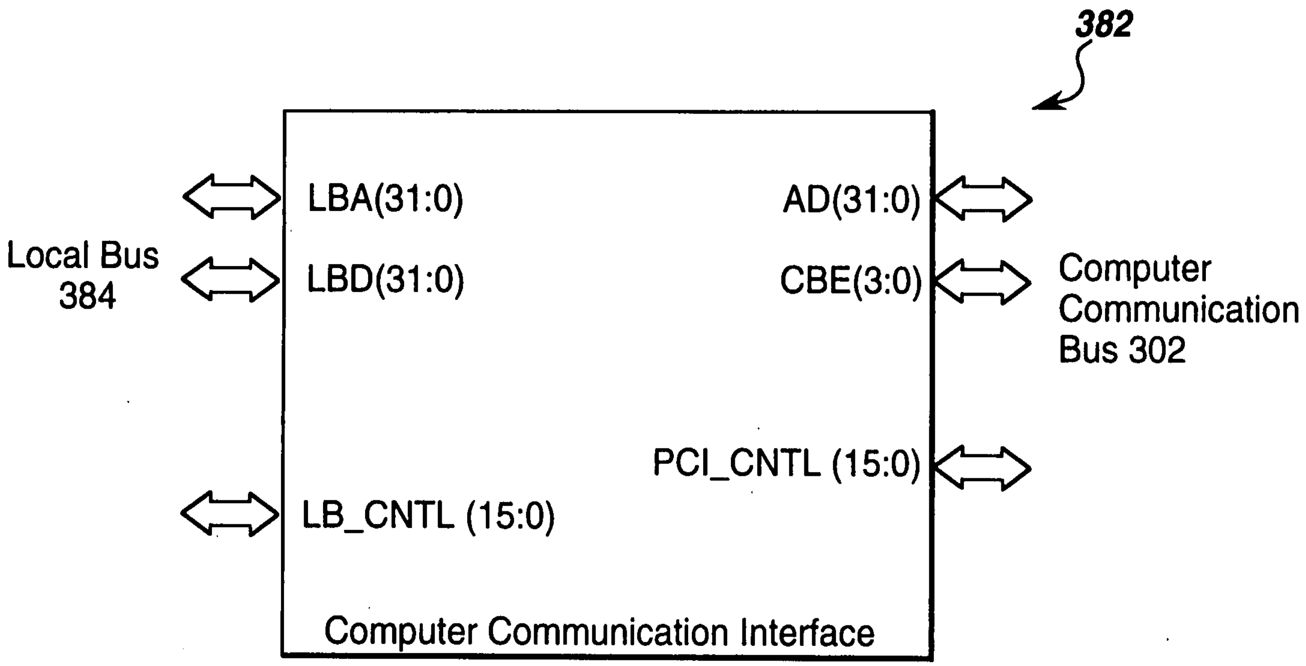

382
Local Bus
384
LBA(31:0)
LBD(31:0)
LB_CNTL (15:0)
AD(31:0)
CBE(3:0)
PCI_CNTL (15:0)
Computer
Communication
Bus 302
Computer Communication Interface

fig. 37

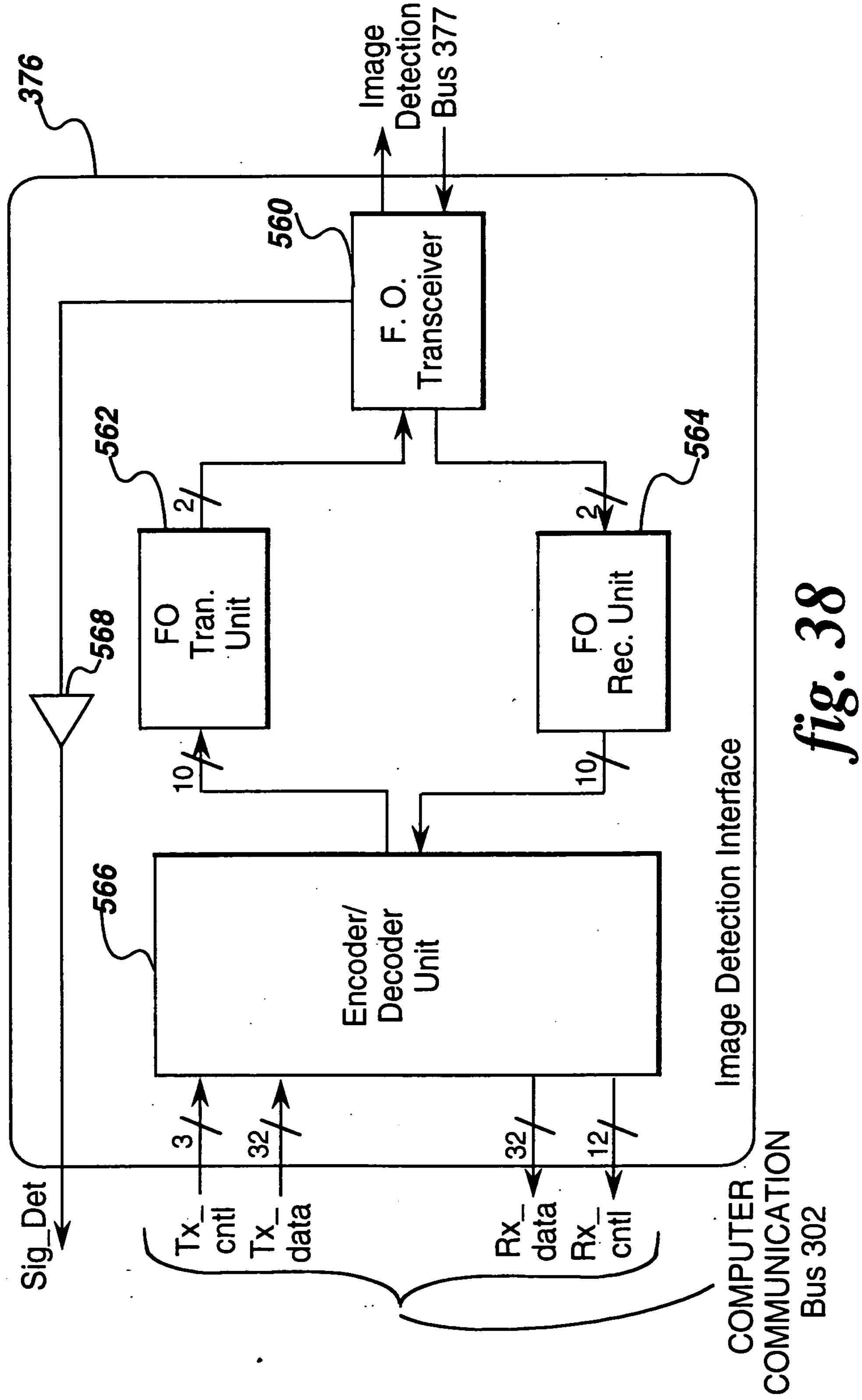

376
Image Detection Bus 377
560
F. O. Transceiver
562
2
FO Tran. Unit
564
2
FO Rec. Unit
568
10
10
566
Encoder/ Decoder Unit
Image Detection Interface
3
32
32
12
Sig_Det
Tx_ cntl
Tx_ data
Rx_ data
Rx_ cntl
COMPUTER COMMUNICATION Bus 302

fig. 38

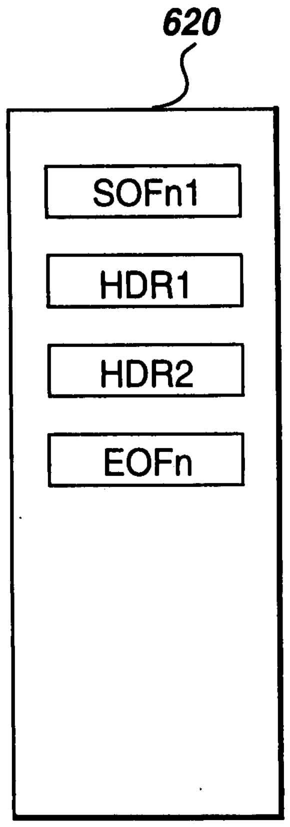


fig. 39

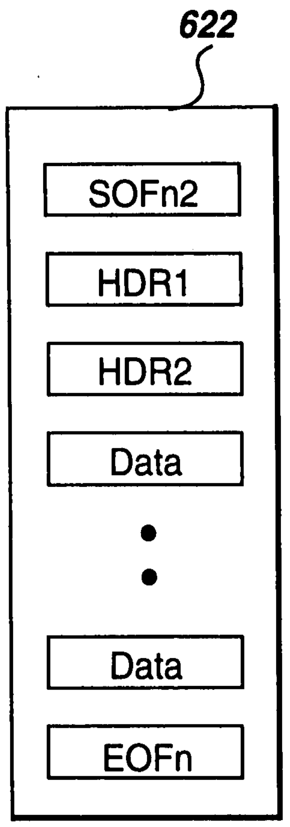


fig. 40

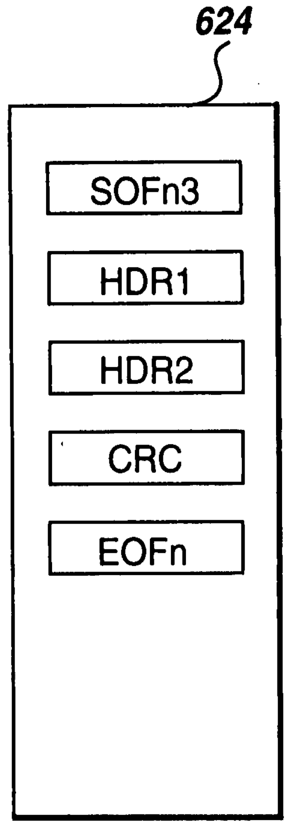


fig. 41

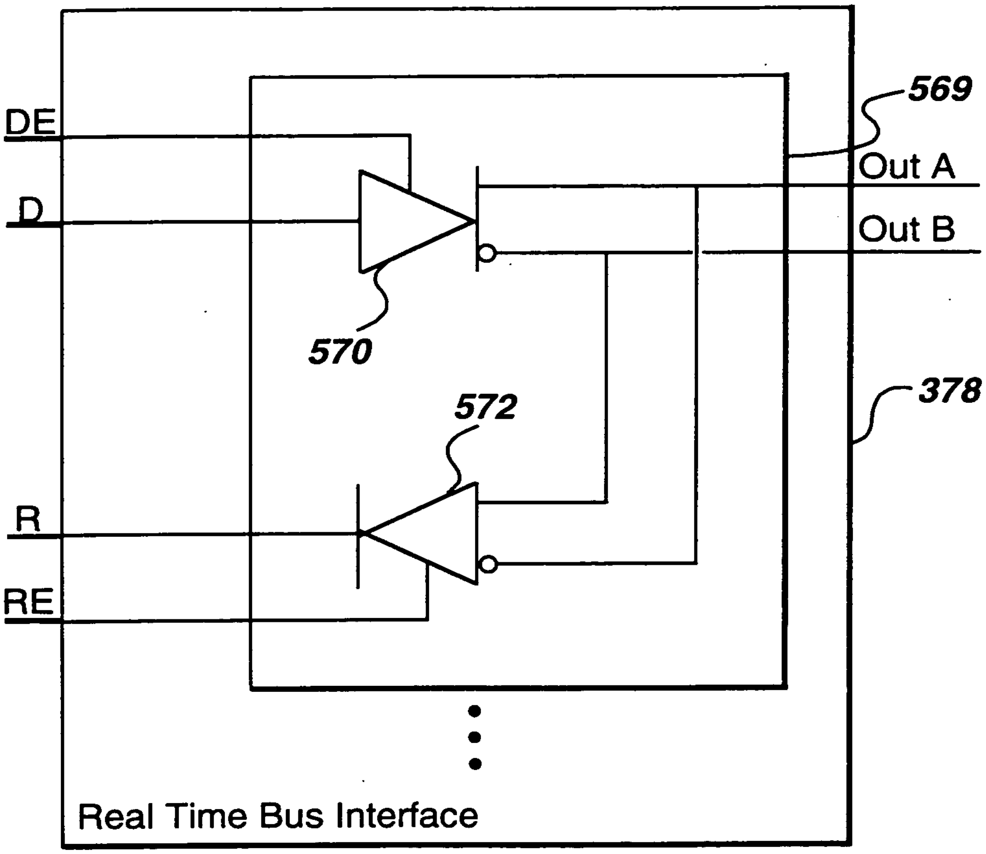


fig. 42

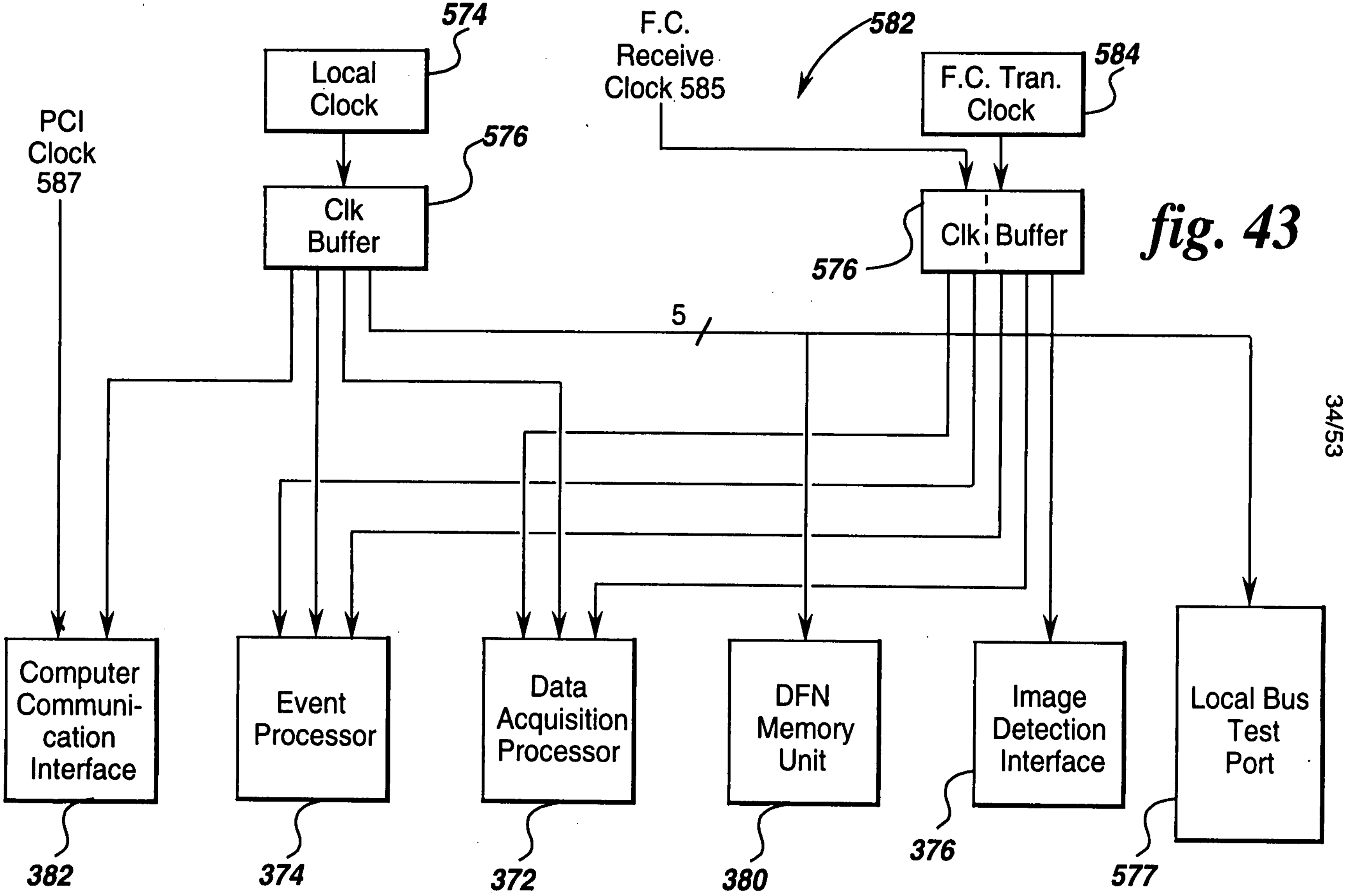

574
Local Clock
576
Clk Buffer
PCI Clock 587
F.C. Receive Clock 585
582
584
F.C. Tran. Clock
576
Clk Buffer
5
Computer Communi-cation Interface
382
Event Processor
374
Data Acquisition Processor
372
DFN Memory Unit
380
Image Detection Interface
376
Local Bus Test Port
577

fig. 43

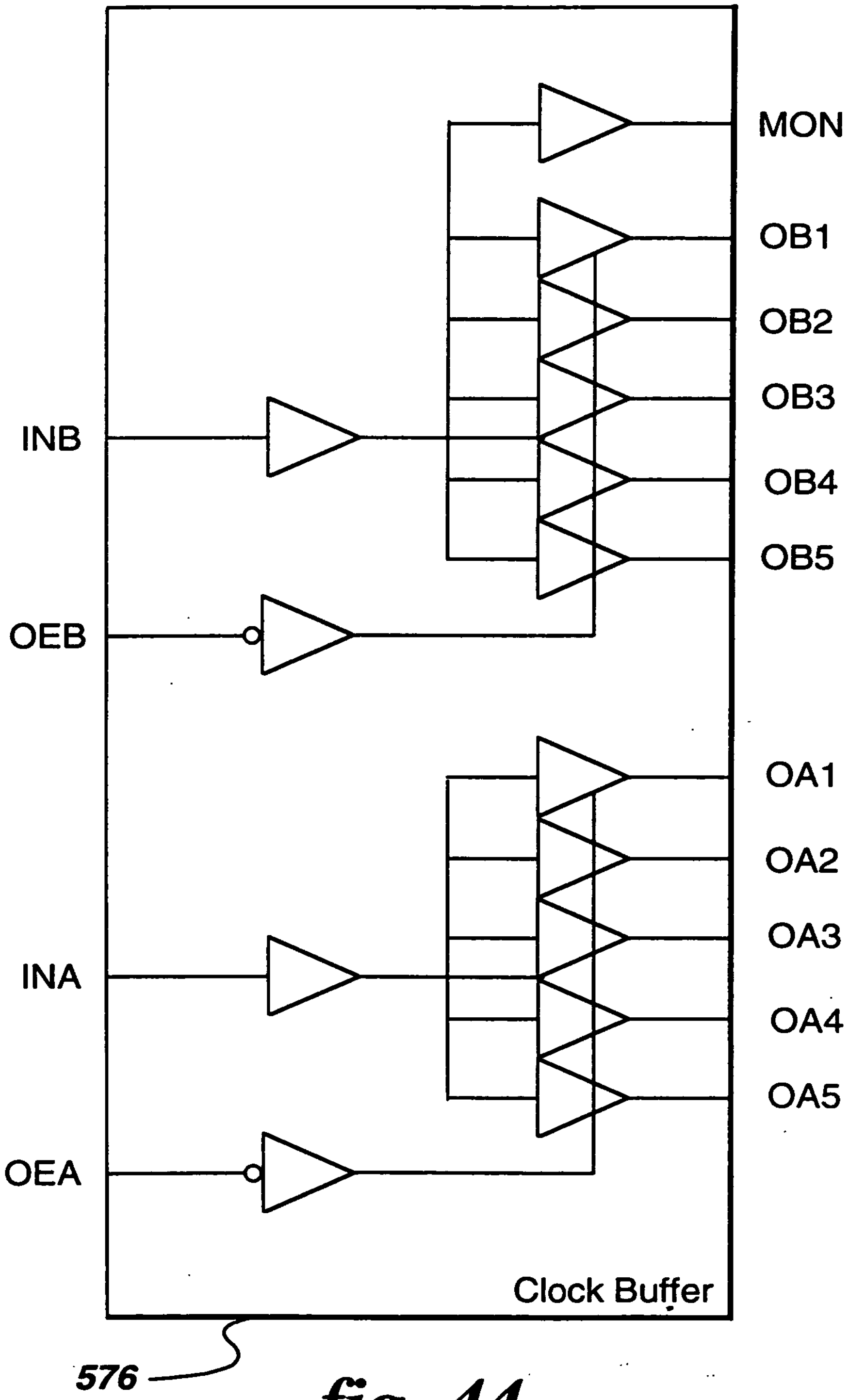

MON
OB1
OB2
OB3
OB4
OB5
INB
OEB
OA1
OA2
OA3
OA4
OA5
INA
OEA
Clock Buffer
576

fig. 44

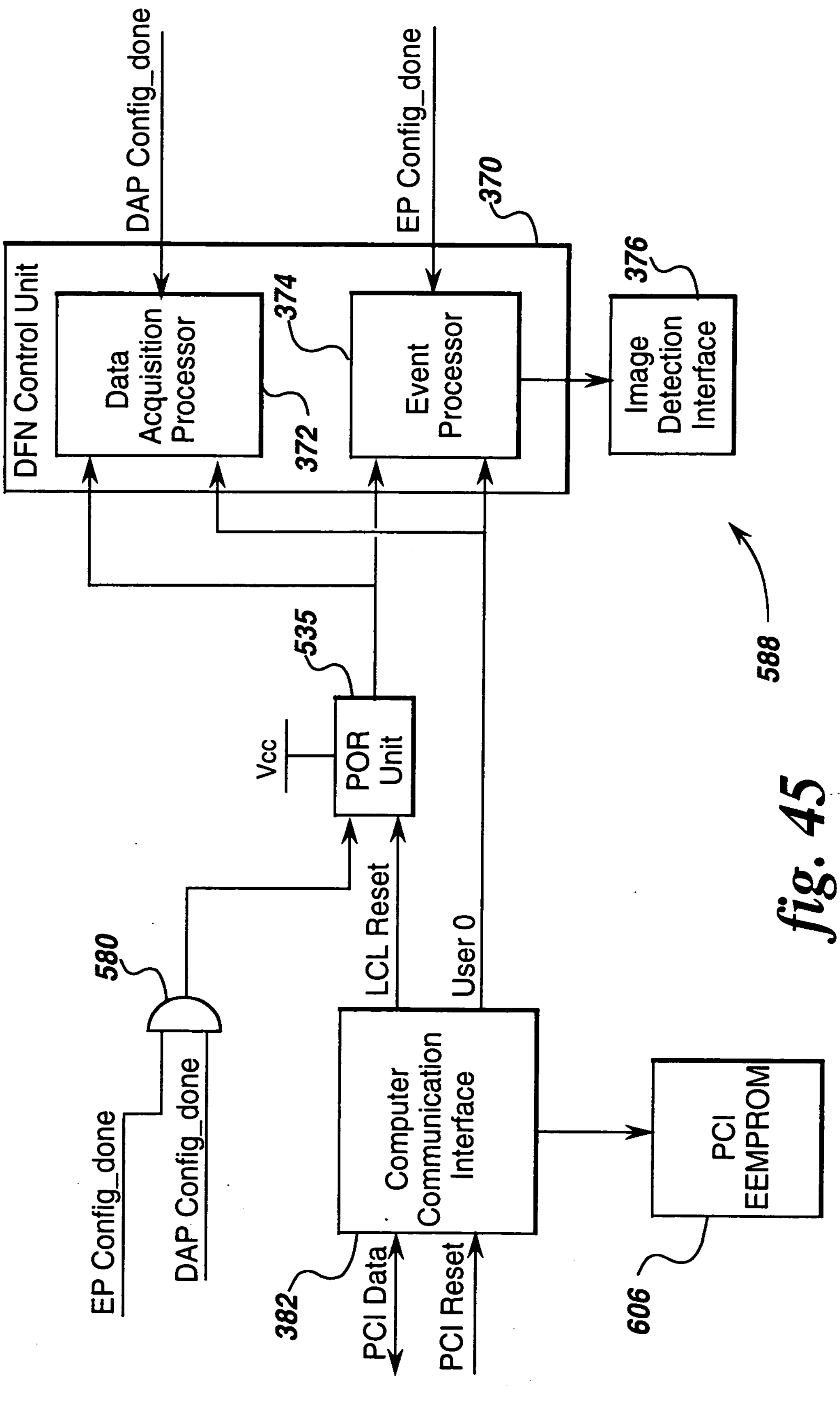

DAP Config_done
EP Config_done
370
DFN Control Unit
Data Acquisition Processor
372
374
Event Processor
376
Image Detection Interface
535
Vcc
POR Unit
588
580
EP Config_done
DAP Config_done
LCL Reset
User 0
Computer Communication Interface
382
PCI Data
PCI Reset
PCI EEMPROM
606

fig. 45

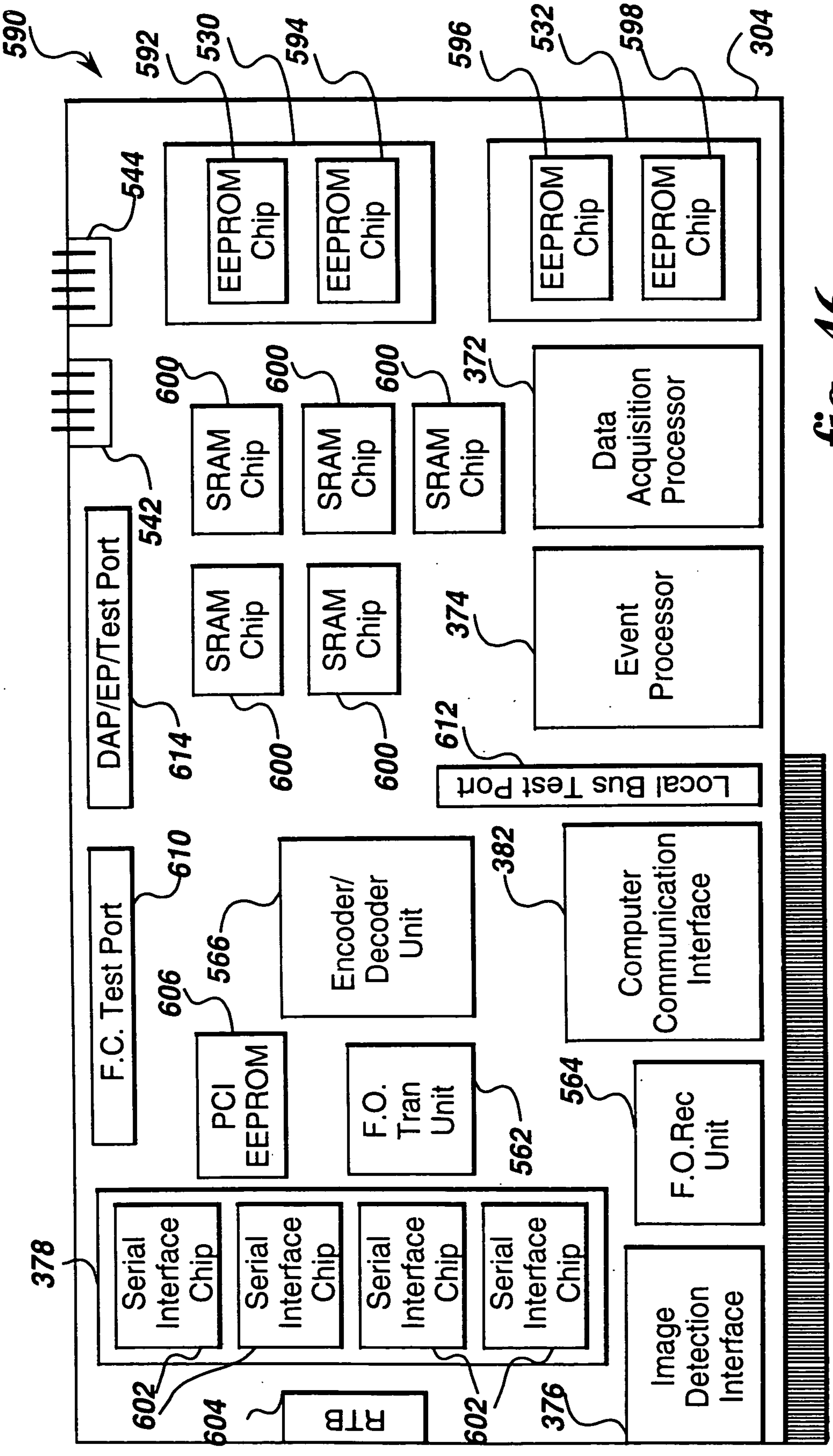
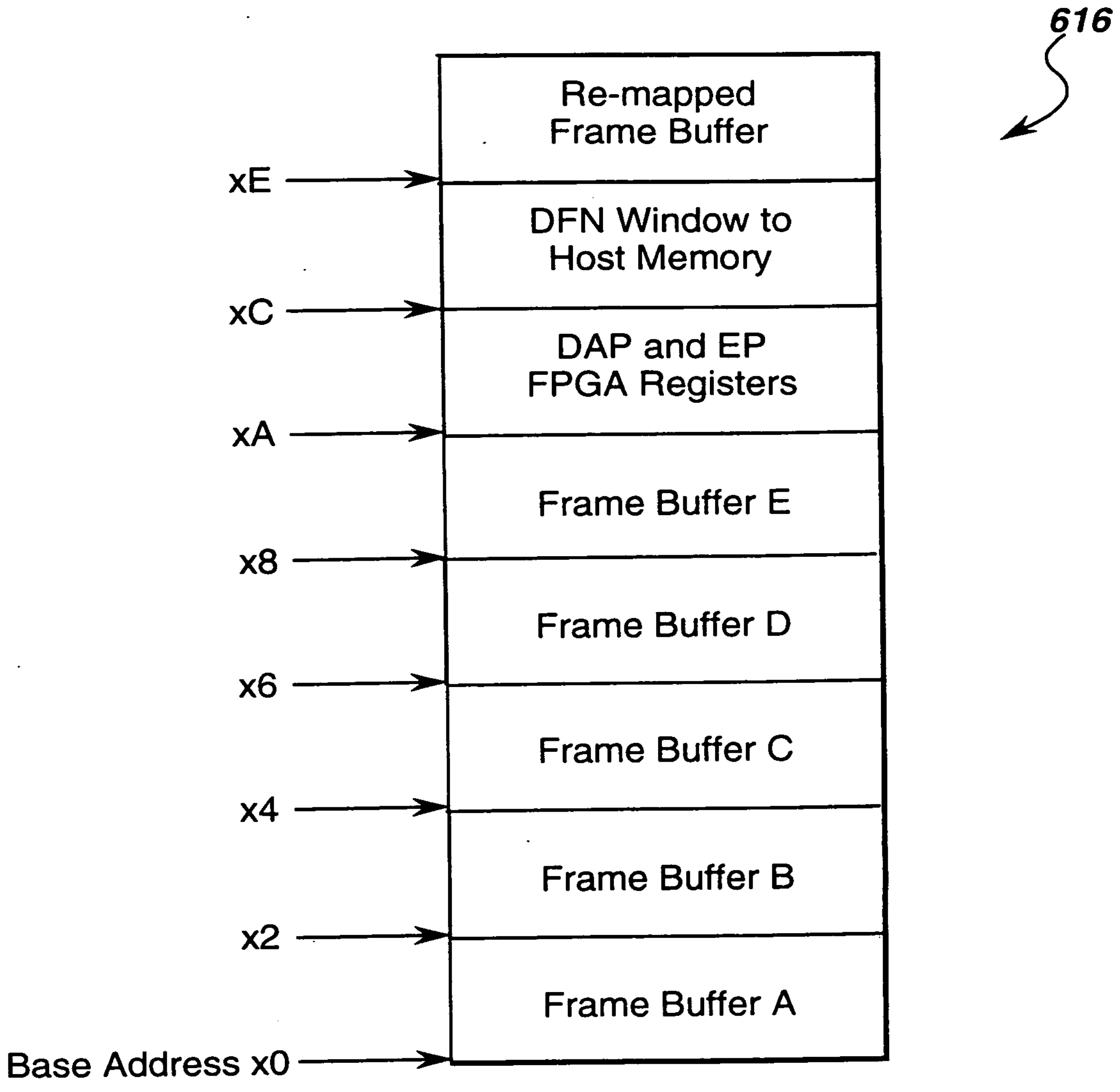

590
592
530
594
596
532
598
304
544
EEPROM Chip
EEPROM Chip
EEPROM Chip
EEPROM Chip
542
600
600
600
372
SRAM Chip
SRAM Chip
SRAM Chip
Data Acquisition Processor
DAP/EP/Test Port
SRAM Chip
SRAM Chip
374
Event Processor
614
600
600
612
Local Bus Test Port
F.C. Test Port
610
Encoder/ Decoder Unit
566
382
Computer Communication Interface
606
PCI EEPROM
F.O. Tran Unit
562
564
F.O.Rec Unit
378
Serial Interface Chip
Serial Interface Chip
Serial Interface Chip
Serial Interface Chip
Image Detection Interface
602
604
RTB
602
376

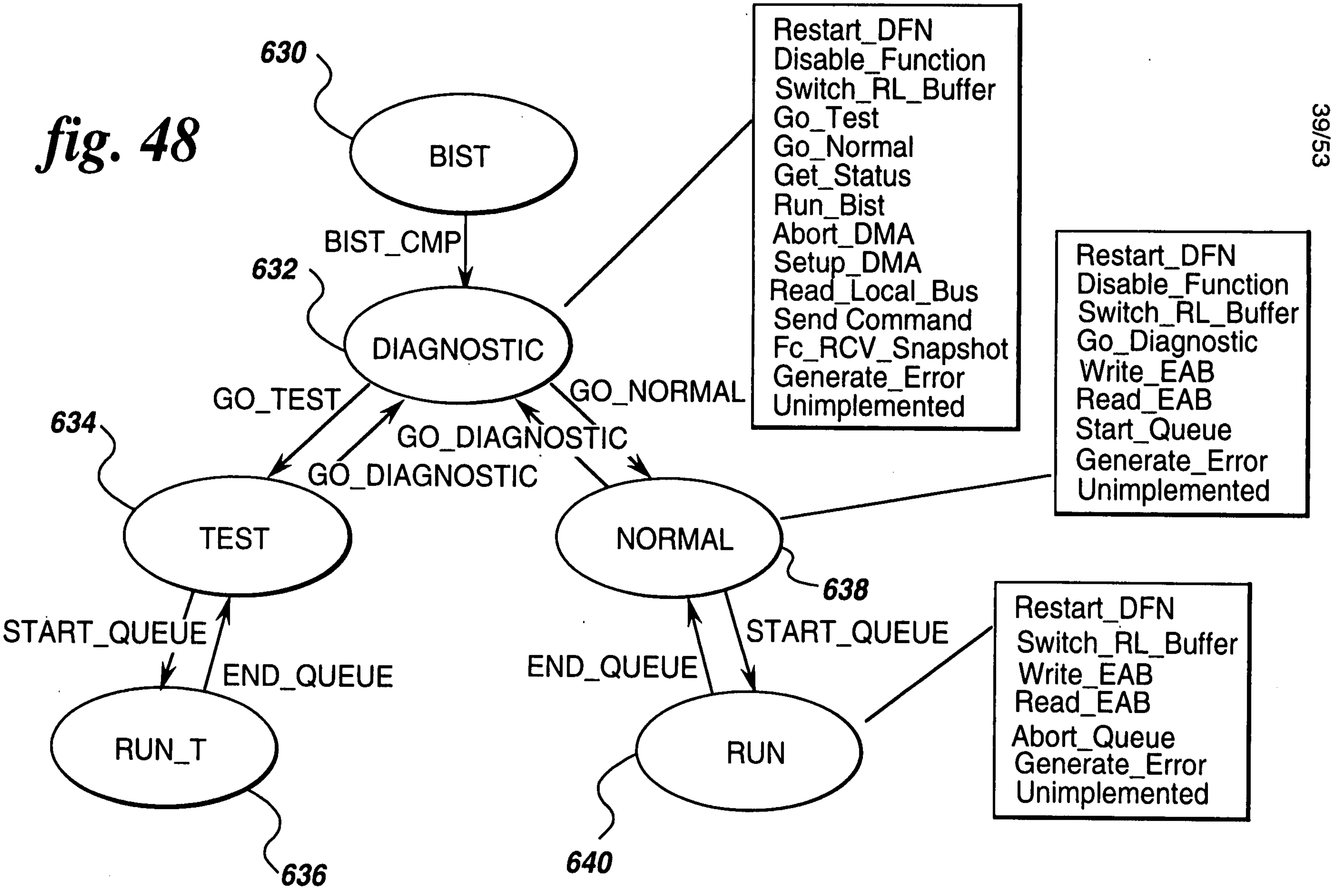
fig. 46



Mapping of 16 MByte PCI Address Space

fig. 47

fig. 48


630
BIST
BIST_CMP
632
DIAGNOSTIC
Restart_DFN
Disable_Function
Switch_RL_Buffer
Go_Test
Go_Normal
Get_Status
Run_Bist
Abort_DMA
Setup_DMA
Read_Local_Bus
Send Command
Fc_RCV_Snapshot
Generate_Error
Unimplemented
GO_TEST
GO_DIAGNOSTIC
GO_DIAGNOSTIC
GO_NORMAL
634
TEST
NORMAL
638
Restart_DFN
Disable_Function
Switch_RL_Buffer
Go_Diagnostic
Write_EAB
Read_EAB
Start_Queue
Generate_Error
Unimplemented
START_QUEUE
END_QUEUE
RUN_T
636
END_QUEUE
START_QUEUE
RUN
640
Restart_DFN
Switch_RL_Buffer
Write_EAB
Read_EAB
Abort_Queue
Generate_Error
Unimplemented

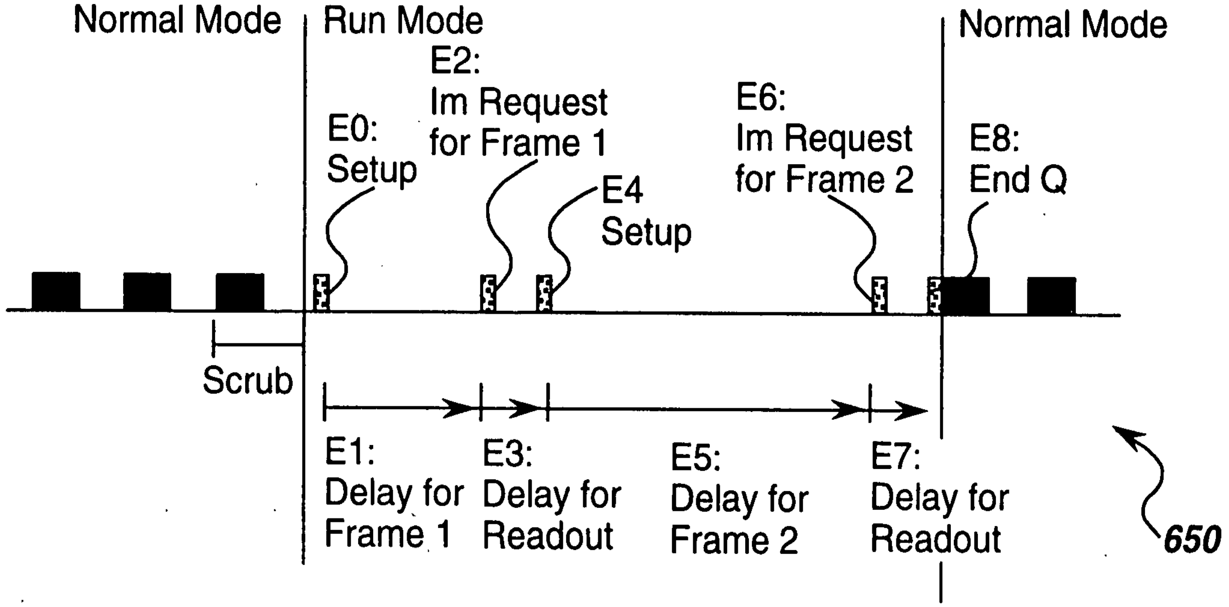

Normal Mode
Run Mode
Normal Mode
E0:
Setup
E2:
Im Request
for Frame 1
E4
Setup
E6:
Im Request
for Frame 2
E8:
End Q
Scrub
E1:
Delay for
Frame 1
E3:
Delay for
Readout
E5:
Delay for
Frame 2
E7:
Delay for
Readout
650

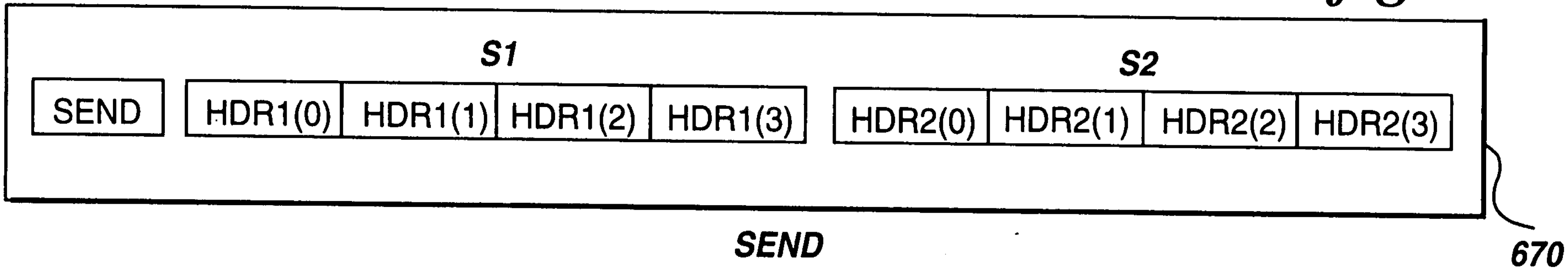
fig. 49

Event Mnemonic	*Event* (showing size of arguments)	*Op Code* (hex)	*Data* (bytes)	*Total* (bytes)
Endq	Endq	14	0	1
Delay (T)	Delay (0xff ff ff ff)	10	4	5
Send (command, value)	Send (0xff ff ff ff, 0xff ff ff ff)	04	8	9
LoopKN (K, N)	LoopKN (0xff ff, 0xff)	0C	3	4
LoopKF (K, F)	LoopKF (0xff ff, 0xff ff ff)	0D	5	6
Wait (F)	Wait (0xff ff, ff)	09	3	4
Flag (F)	Flag (0xff ff, ff)	08	3	4

660

fig. 50

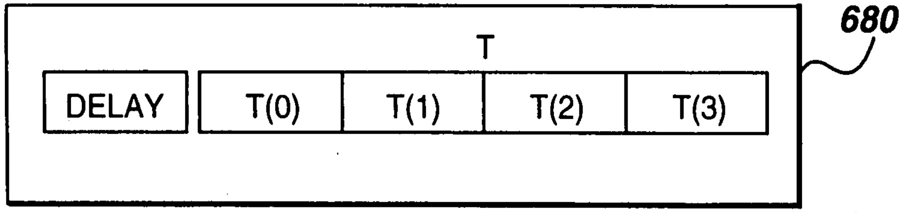
fig. 51



Error Mnemonic	*Description of Error*
FC_TIMEOUT	Timeout Expired With No ACK Detected
FC_BAD_ACK	ACK Did Not Match Transmitted Command
FC_EXTRA_ACK	Unexpected ACK Received
FC_EXTRA_CMD	New Send Event While Waiting for ACK From Previous Send
SIG_DETN	No Input Signal Power on Fibre Channel (Cable Disconnected?)
RXERROR	Fibre Channel Receiver Detected Bad Data (Defective Chipset?)
WRDSYNCN	Fibre Channel Data Link Unsynchronized
CRXS(1)	Bad Received CRC Detected (Fiber-optic Cable Problem?)
CRXS(3) & CRXS(2)	Bad Order in Link State Machine (Defective Chipset?)

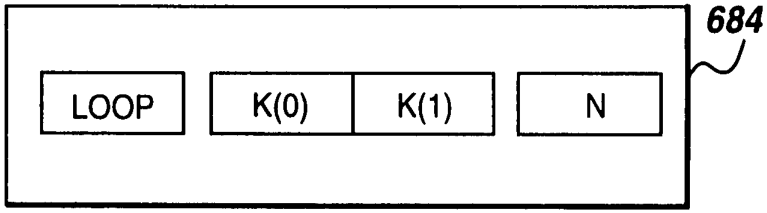
672

fig. 52



DELAY T

fig. 53



LOOP KN

fig. 54

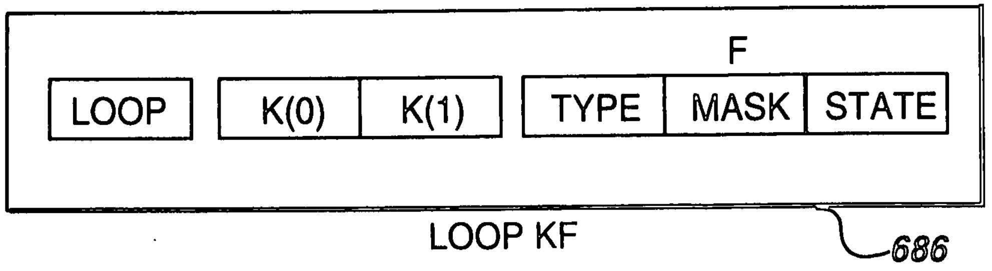


fig. 55

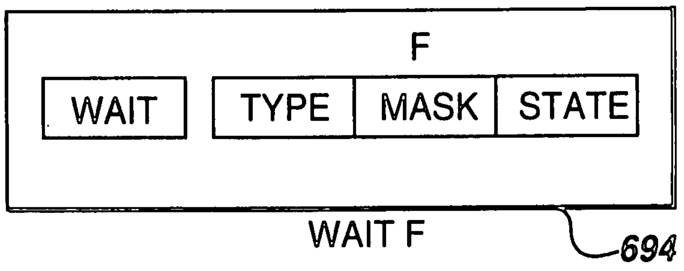


fig. 56

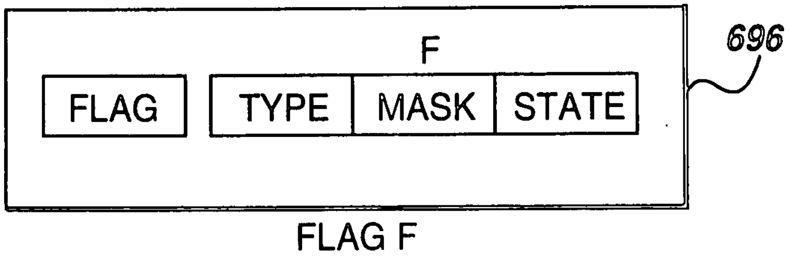


fig. 57

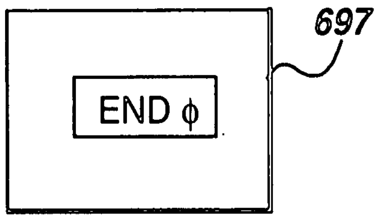


fig. 58

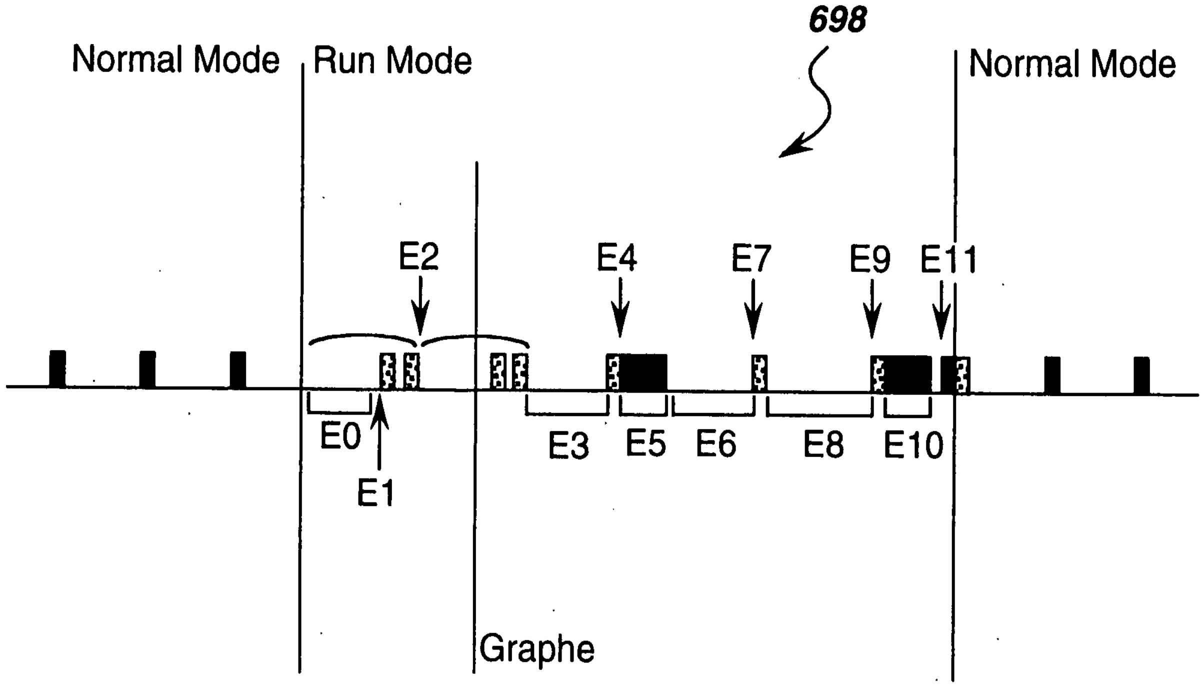

698
Normal Mode
Run Mode
Normal Mode
E2
E4
E7
E9
E11
E0
E1
E3
E5
E6
E8
E10
Graphe

fig. 59

E11	EndQ
E10	Delay 125 ms
E9	Send Im Request
E8	Delay 500 ms
E7	Flag RT2
E6	Delay 50 ms
E5	Delay 125 ms
E4	Send Im Request
E3	Delay 300 ms
E2	Loop 2, RT1
E1	Send Scrub
E0	Delay 300 ms

700

EVENT QUEUE

fig. 60

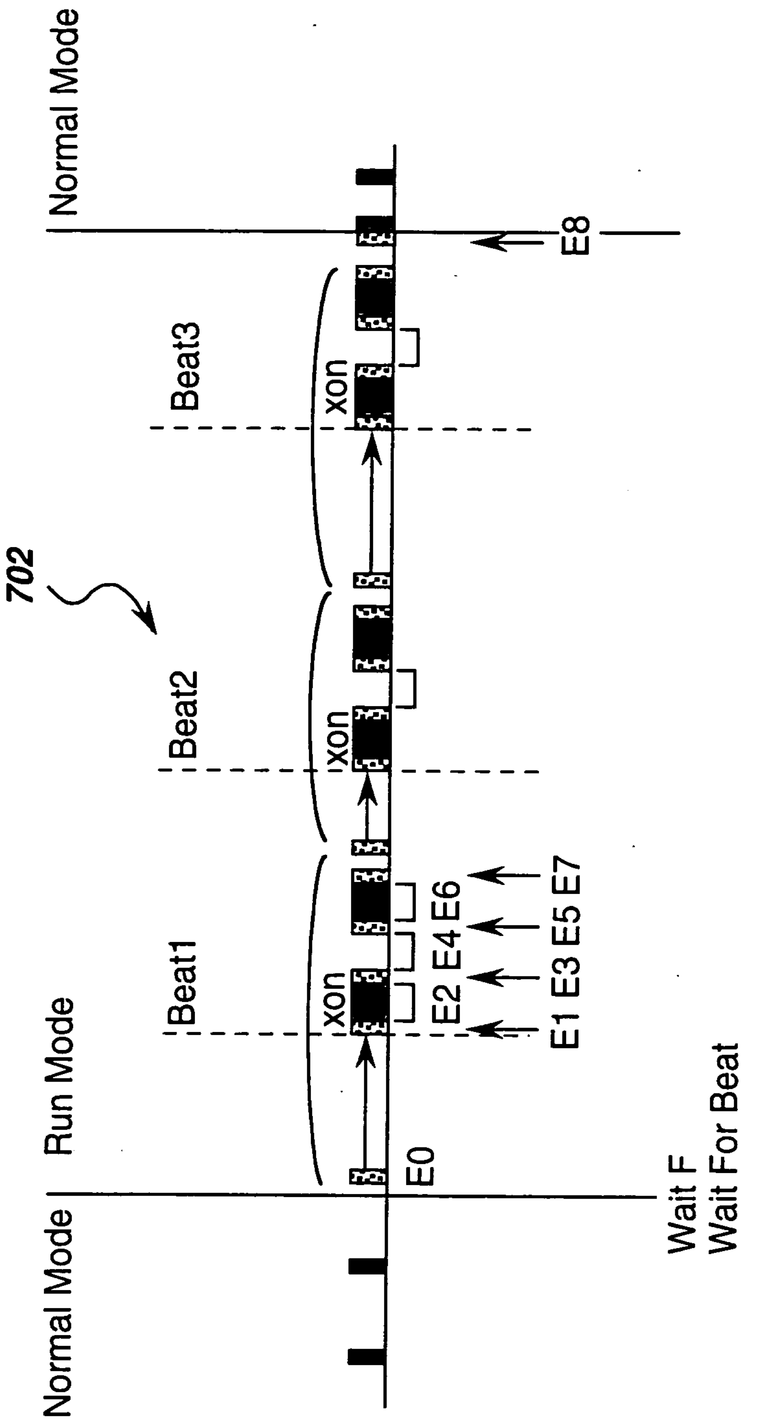
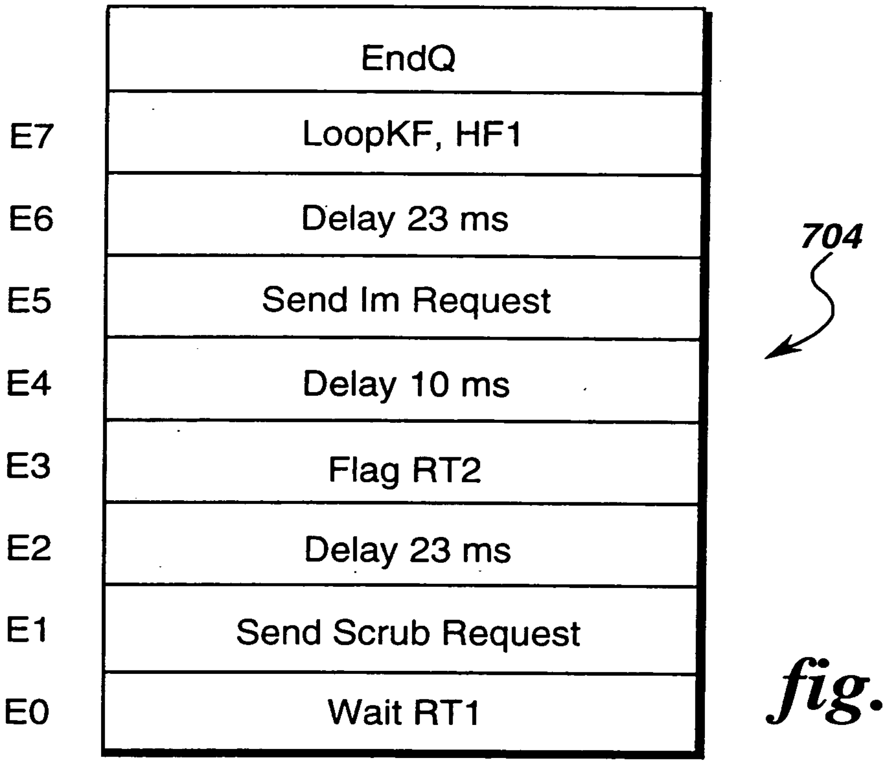

Normal Mode
Run Mode
Normal Mode
702
Beat1
Beat2
Beat3
xon
xon
xon
E0
E1 E3 E5 E7
E2 E4 E6
E8
Wait F
Wait For Beat

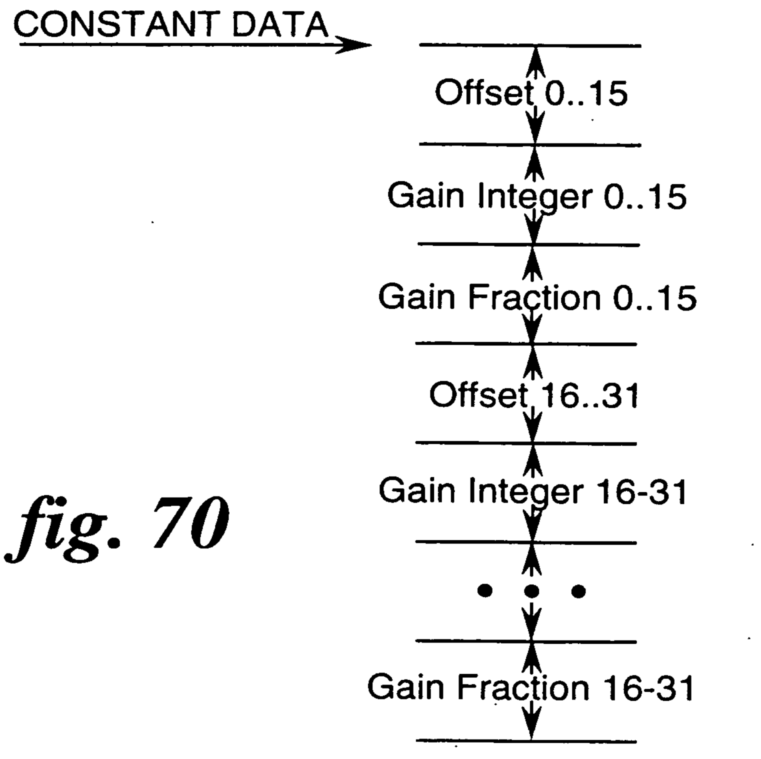
fig. 61



	EndQ
E7	LoopKF, HF1
E6	Delay 23 ms
E5	Send Im Request
E4	Delay 10 ms
E3	Flag RT2
E2	Delay 23 ms
E1	Send Scrub Request
E0	Wait RT1

EVENT QUEUE

fig. 62



Constant Memory Format

fig. 70

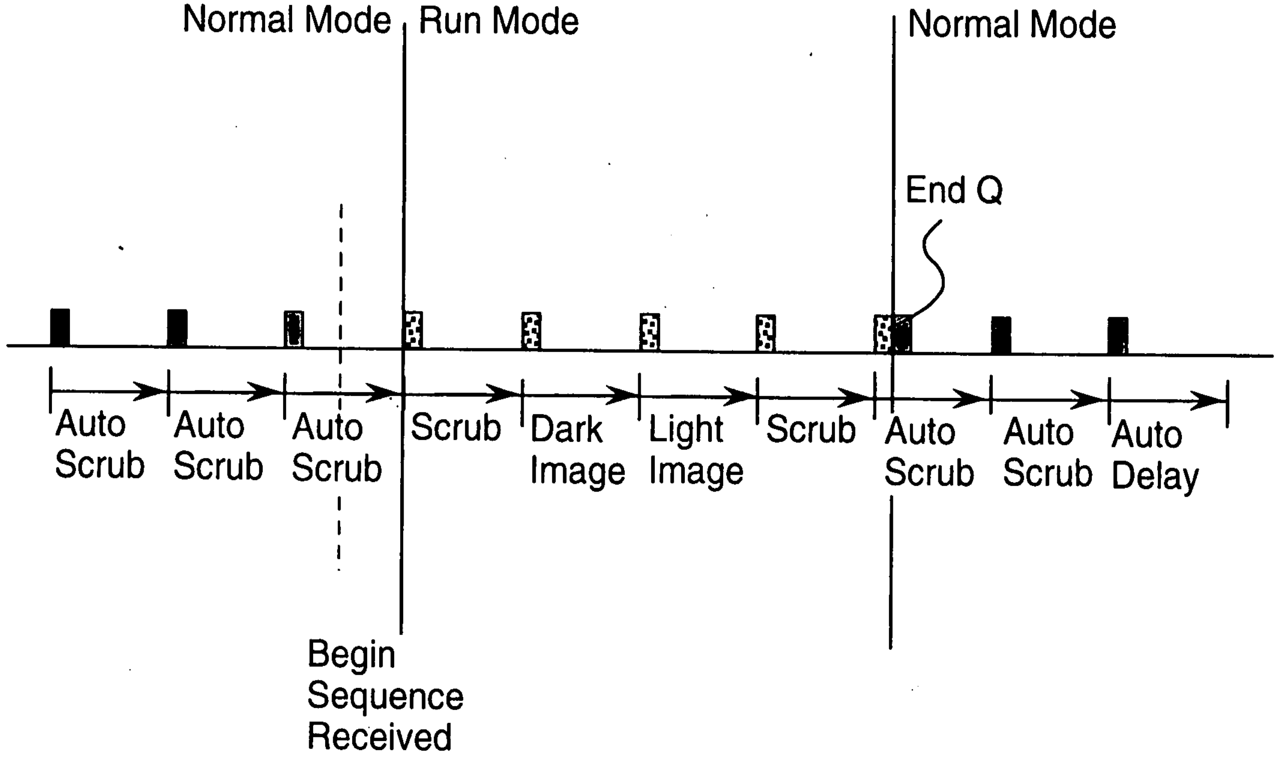

Normal Mode
Run Mode
Normal Mode
End Q
Auto Scrub
Auto Scrub
Auto Scrub
Scrub
Dark Image
Light Image
Scrub
Auto Scrub
Auto Scrub
Auto Delay
Begin Sequence Received

fig. 63

```
 sequence_begin ( );
 # define qv defaults:
%qv1 =('delay_qv' => 5000);
# call frame with qv's
frame_type1(NULL, \%qv1, 1);
  sequence_end ( );
```

fig. 64

```
sub frame
{
$QVf  = 'frame' ;
%qv = ('delay_qv' = > [10000]);
%qp = ( );
compile_init (@_,\%qp, \%qv, $QVf);
      Delay('Delay_qv1');
compile_finit ( );
}
```

fig. 65

```
pDFN->DFNChangeQueueVariable
(
(char *) SymName,                          // variable name
(char *) sndBuf,                           // new value
BufSize                                    // num bytes to write
  (ULONG *) & Debug                        // developer info
);
```

fig. 66

```
// load and run the event sequence
pDFNBeginSequenceNoMappingNoLog
      (snum,"d:\\HF.bin") ;
// assign data to be passed
sndBuf = 25000;
// change the queue variable
pDFN->DFNChange QueueVariable
(
 (char *) SymName,              // variable name
 (char *) sndBuf,               // new value
 (ULONG ) sizeof sndBuf         // num bytes to write
 (ULONG *) & debug              // developer info
);
```

fig. 67

```
sub frame_type1
{
 $HFfrm = 'frame_type1';
 %qv = ('delay_qv' = > [20000]);
 %qp = ( );
 $image_cmd  = [0x800000,0x0];
 compile_init (@_,\%qp, \%qv, $HFfrm);
   Send ( $image_cmd);
    Delay('delay_qv');
    LoopKF(2, 0xAAFF01);
   compile_finit( ) ;
}
```

fig. 68

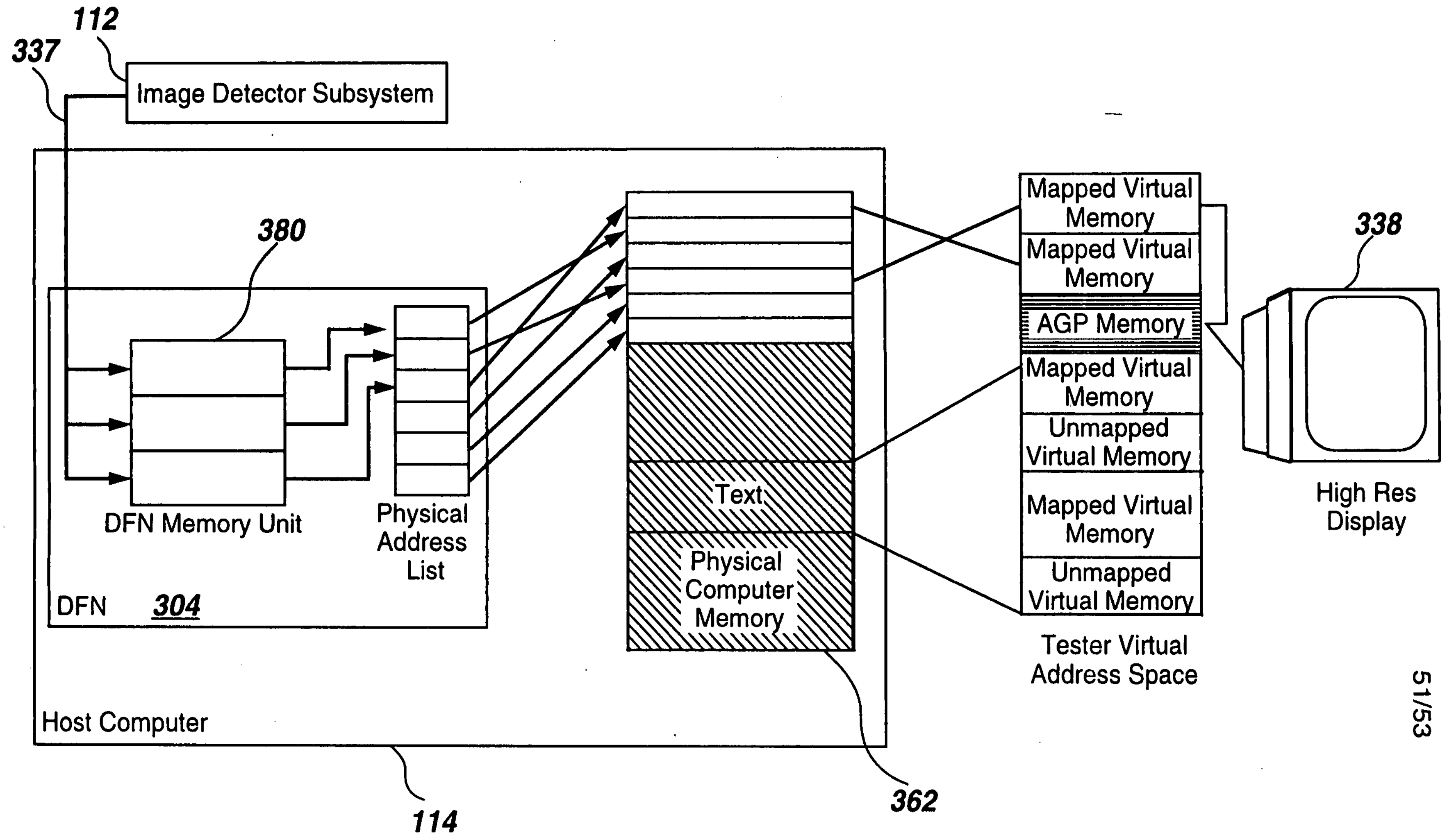

337
112
Image Detector Subsystem
380
DFN Memory Unit
Physical Address List
DFN
304
Host Computer
114
Text
Physical Computer Memory
362
Mapped Virtual Memory
Mapped Virtual Memory
AGP Memory
Mapped Virtual Memory
Unmapped Virtual Memory
Mapped Virtual Memory
Unmapped Virtual Memory
Tester Virtual Address Space
338
High Res Display

fig. 69

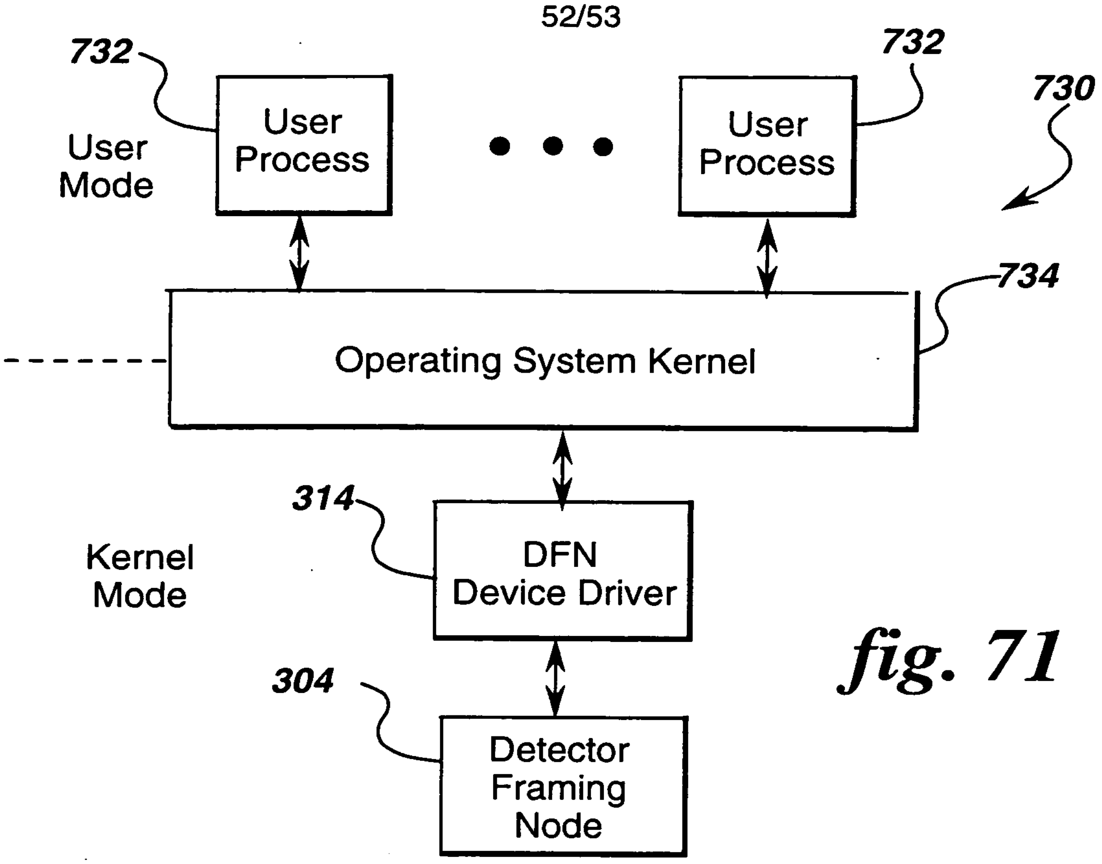

732
User Process
• • •
732
User Process
730
User Mode
734
Operating System Kernel
314
DFN Device Driver
Kernel Mode
304
Detector Framing Node

fig. 71

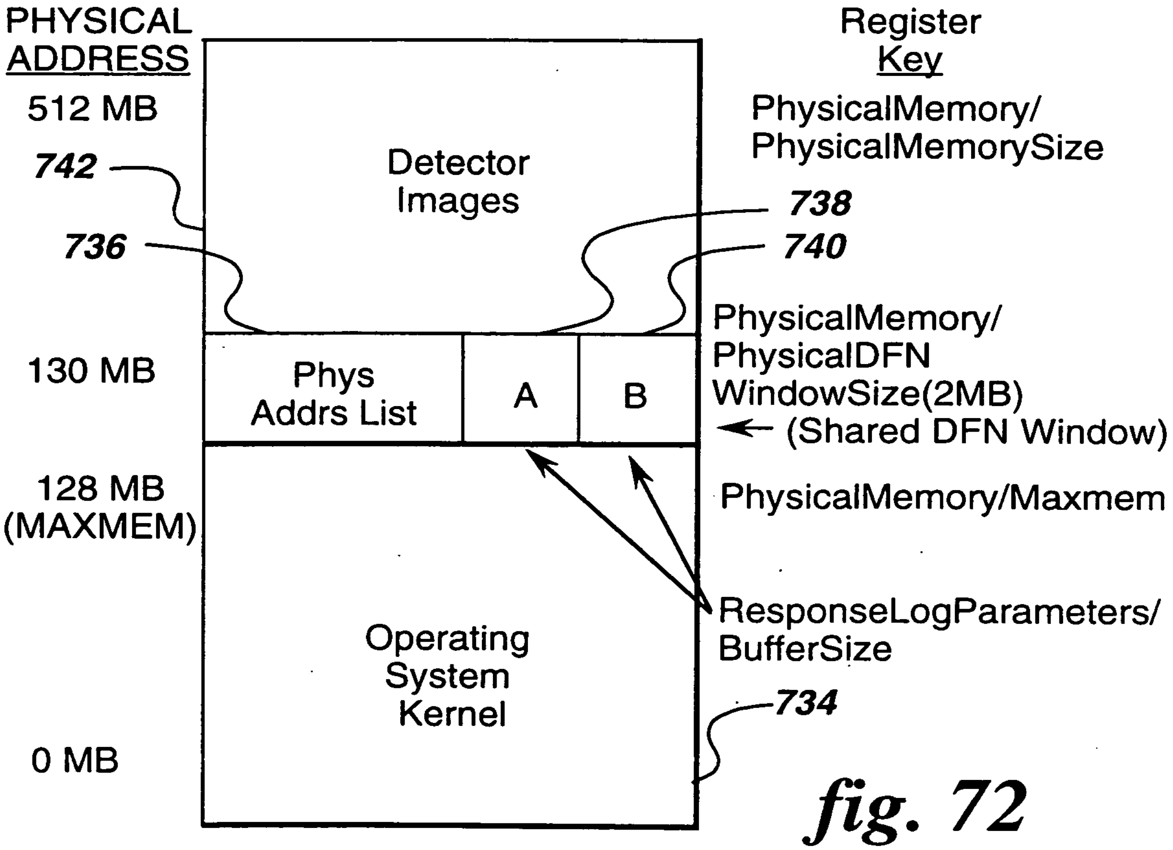

PHYSICAL ADDRESS
512 MB
742
736
130 MB
128 MB (MAXMEM)
0 MB
Detector Images
Phys Addrs List
A
B
Operating System Kernel
Register Key
PhysicalMemory/ PhysicalMemorySize
738
740
PhysicalMemory/ PhysicalDFN WindowSize(2MB)
(Shared DFN Window)
PhysicalMemory/Maxmem
ResponseLogParameters/ BufferSize
734

fig. 72

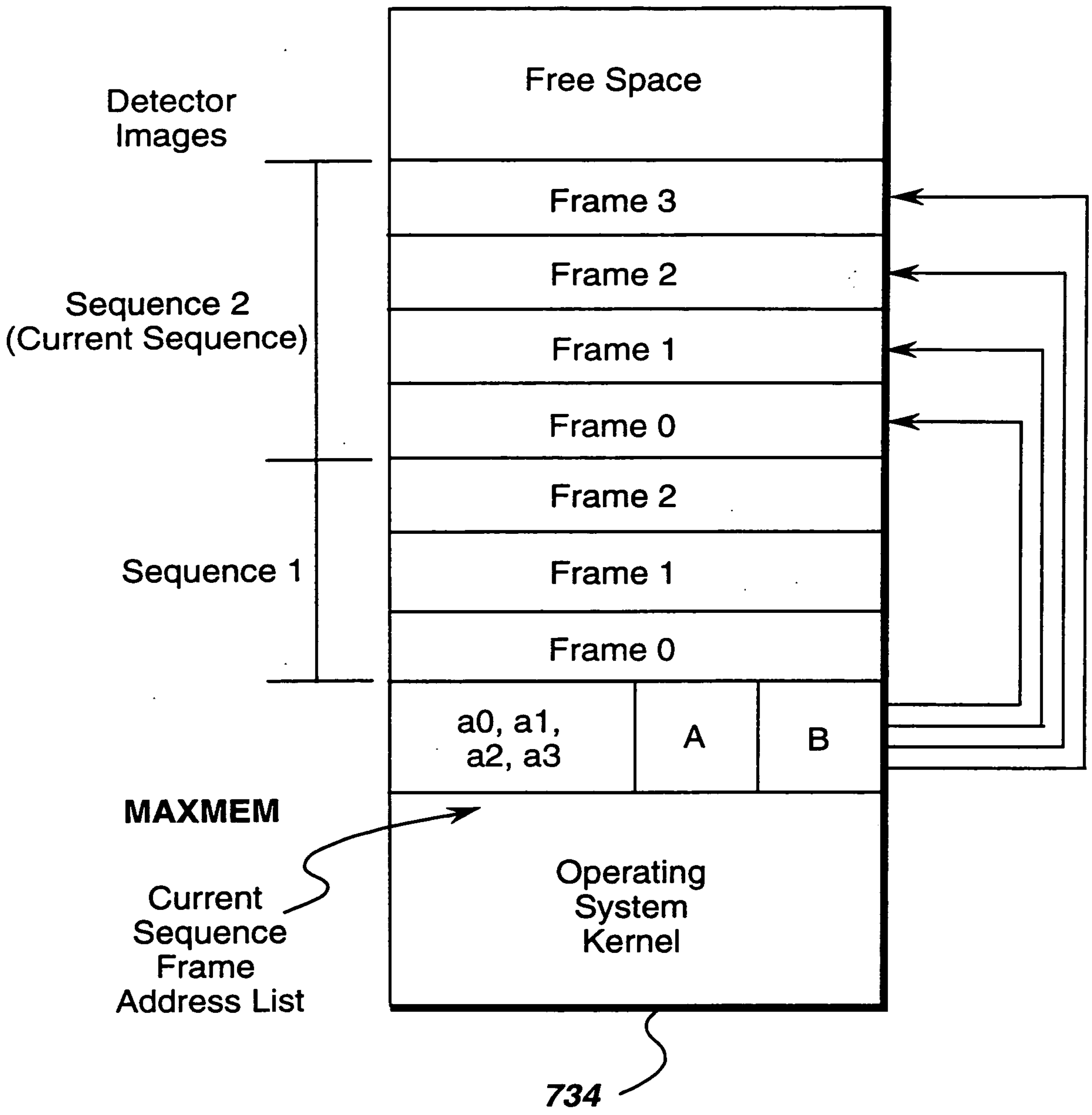

Detector
Images
Free Space
Frame 3
Frame 2
Sequence 2
(Current Sequence)
Frame 1
Frame 0
Frame 2
Sequence 1
Frame 1
Frame 0
a0, a1,
a2, a3
A
B
MAXMEM
Current
Sequence
Frame
Address List
Operating
System
Kernel
734

fig. 73